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Robust Feedback Linearization Control for DAB Converter feeding a CPL

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Abstract: Cascaded converters are used to satisfy the different voltage levels that loads need. Instability problems in cascaded systems may occur due to the interaction of Point-of-Load (POL) converters. POL converters exhibit the important characteristic of almost-perfect regulation at the output terminals independent of the input perturbations. However, such characteristic reflects at the input terminal as a constant power load (CPL). CPL exhibits incremental negative resistance behavior causing undesired oscillations and a high risk of instability in interconnected converters. In this paper, the cascaded converter system consists of a Dual Active Bridge (DAB) DC-DC converter that maintains a regulated DC voltage on the intermediate bus and a POL DC-DC Buck converter that acts as a CPL. Aiming to ensure system stability and effectively mitigate oscillations effects in a cascaded system, this paper proposes a Robust Feedback Linearization Control to regulate the intermediate DC bus voltage. Simulation tests are performed by using a MATLAB/Simulink simulator to show the robustness and effectiveness of the proposed controller. The simulation results show that the proposed control approach ensures robust control performance and stability with a minor performance degradation compared to a Robust Control approach, Feedback Linearization Control approach, and Classical Control approach.

Keywords: cascaded system, constant power load, dc-dc converter, dual active bridge converter, feedback linearization control, robust control.

1. INTRODUCTION

In recent years, the advancement of power electronic systems has lead to significant evolution in many industrial applications such as microgrid, electric vehicles, renewable energy, energy storage system, power electronic transformers, transmission and distribution systems (Hossain et al., 2018).

In the above applications, a set of converters are used to supply energy from the sources into the DC bus voltage and another set of converters to transfer energy from the DC bus voltage to the loads (Singh et al., 2017; Tahim et al., 2015). These system are known as cascaded power electronic converters that employ point-of-load (POL) converters for power conditioning and voltage regulation (Lucas et al., 2019a). However, POL converters acts as a Constant Power Load (CPL) due to their regulation capability. CPL exhibit negative incremental impedance, which introduces undesired oscillations that may degrade the stability margin or even destabilize the cascaded system even though, each stage is well designed for stand-alone operation (Tahim et al., 2015; Lucas et al., 2019c).

To cope with the undesired effects of the CPL, many studies have been carried out focusing on modeling, stability analysis, and control strategies for a single converter with CPLs (Dragicevic et al., 2016; Mosskull, 2017; Marx et al., 2012; Al-Nussairi et al., 2017). Different topologies of DC-DC converters loaded with CPLs and their feedback control loops have been analyzed in the literature. One of the most common approaches to overcome the negative incremental impedance problem is by passive damping (Mosskull, 2017; Cespedes et al., 2011). Passive-damping methods can avoid instability by effectively converting a CPL into a resistive load. However, the problem with passive-damping methods are their effect on systems size, weight, cost and efficiency, in addition, they add limitations to the design (Li et al., 2012).

Other methods are active techniques, which can be applied on the load side and on the generation side. In Wu and Lu (2015), an active damping control technique is proposed, which emulates a virtual resistance in parallel to the CPL. In Zhang et al. (2016), the authors propose an active damping method by adding a virtual RLC circuit into

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the LC input filter to avoid the power loss of the passive components via changing the control block of the CPL. However, these active damping methods affect the power quality of the system.

Sliding-mode control (SMC) is a large-signal time-domain analytical technique for controlling the dynamic behavior of switching systems that has been used for stabilizing DC-DC converters and mitigating CPL-based instabilities in the last years (Zhao et al., 2014; Benadero et al., 2015).

Model-predictive control (MPC) has also been introduced to mitigate the instability caused by CPL into multiconverter systems. MPC controls the variation of the intermediate DC bus and modifies the load impedance which is seen at the point of common coupling (Dragicevic, 2018; Mardani et al., 2019).

Robust control techniques have been considered for the elementary power electronics switching converters with a CPL to cope with the mentioned CPL instability (Lucas et al., 2019a,c; Vafamand et al., 2019). Lucas et al. (2019a,c) proposes a robust control approach that takes into account the uncertainties of the system from the outset in the controller design process, then, the LMI optimization problem, which adjusts the parameters of the robust controller, is solved by convex optimization using the Linear programming approach, Kharitonov Theorem and Chebyshev Theorem. These proposed controllers ensure robust performance and stability, and providing a better control performance in comparison with a classical controller.

Feedback linearization control (FLC) aims to compensate the nonlinearity introduced by CPL and stabilize the system. FLC is generally based on finding a nonlinear feedback, which cancels the nonlinearity. Consequently, control system can be designed using conventional linear control theory (Singh et al., 2017). Rahimi et al. (2010) proposes a loop-cancellation technique to stabilize all basic DC-DC converters feeding a resistive and CPL using suitable nonlinear feedback, which cancels nonlinearity introduced due to the presence of CPL. In Solsona et al. (2015), the authors implement feedback linearization using a coordinate transform for a pure CPL with a full-order feedback controller. In Xu et al. (2019), a novel composite nonlinear controller is presented where efficient estimation is obtained using a nonlinear disturbance observer in the presence of the load power variation within a fast dynamic response.

In this context, this paper proposes a Robust feedback linearization control approach to mitigate the destabilizing effect of CPL in a cascaded converter system. The cascaded system comprised of a Dual Active Bridge (DAB) DC-DC converter (source converter) that regulates the intermediate DC bus voltage and a POL DC-DC buck converter that acts as a CPL, i.e., it transforms the intermediate DC bus voltage to tightly regulated output for the load.

To the best of the authors' knowledge, studies reporting control approaches to mitigate oscillations effects caused by CPL in a cascaded converter system comprised of a DAB DC-DC converter feeding a CPL are still scarce in literature. Recently, Cupelli et al. (2019) addressed an outstanding contribution for the current state-of-the-art on the study of the control of DAB source-side converters in an MVdc microgrid under the influence of CPLs.

In this work, the DAB converter is controlled by single phase-shift-modulation with a fixed duty cycle. Therefore, the proposed controller considers a control scheme based on single-phase-shift (SPS) control.

The proposed robust FLC approach ensures robust performance and stability, and providing a better control performance in comparison with a robust control approach proposed by Lucas et al. (2019b), a classical FLC approach, and a classical control approach based on pole-placement. All the experiments are performed with simulations in Matlab/Simulink.

The Integral of Squared Error (ISE) and the Integral of Time multiply Absolute Error (ITAE) performance indices are computed to analyze the control methodologies compared in this work. The results show the proposed methodology outperforms the other approaches.

The remainder of this paper is organized as follows. Section 2 introduces the description of the system with its instability problem. Section 3 presents the proposed control methodology for designing nonlinear robust controller. Section 4 presents the design of the controllers used in this work. Section 5 describes the experiments to be performed in this paper and also presents the assessment of the simulation results. Finally, Section 6 presents the main conclusions.

2. SYSTEM DESCRIPTION AND PROBLEM FORMULATION

Fig. 1 presents a typical cascaded converter system. The design parameters of the DAB converter and the POL buck converter are given in Table 1.

Table 1. Parameters of the cascaded system

Par.	Unit	Var. (%)	Nom. Val.	Description
DAB Converter				
V_i	V	15	800	Source input voltage
V_{dc}	V		400	DC bus voltage
L_r	mH		1.10	Auxiliary inductor
C_o	μF		104.17	Output Capacitor
D_φ	rad		$\pi/6$	Nominal phase-shift
f_{sw}	kHz		20	Switching frequency
N_2/N_1			0.50	Transformer turn ratio
POL Buck Converter				
V_o	V		200	Output voltage
P_o	W	50	2000	Output power
f_{sw2}	kHz		100	Switching frequency
L_1	mH		10	Filter inductor
C_1	μF		50	Output Capacitor
R_L	Ω		20	Resistance load

The DAB DC-DC converter regulates the DC voltage level on the DC bus (v_{dc}) maintaining the stability of the cascaded converter system.

On the other hand, the POL buck converter exhibits the important characteristic of almost-perfect regulation at

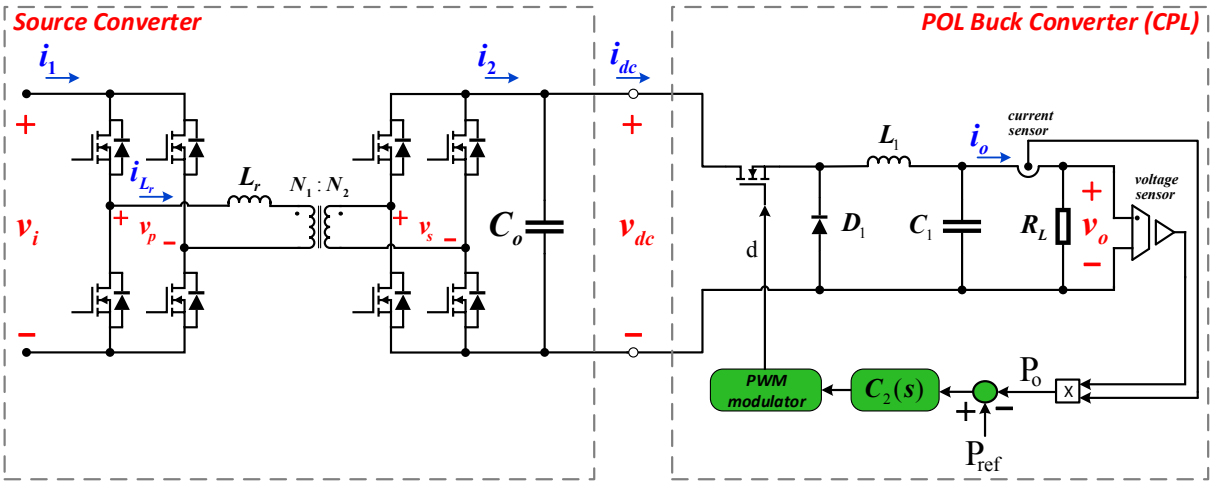
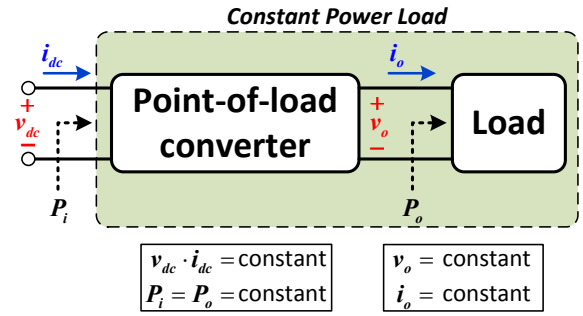
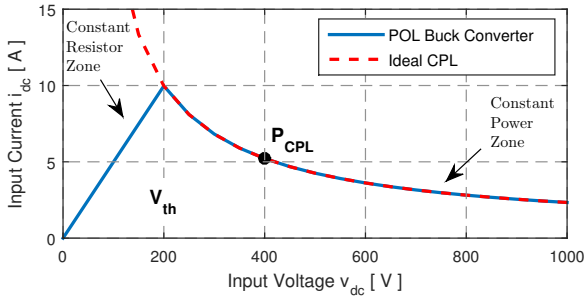


Fig. 1. Circuit diagram of a cascaded converter system.

the output terminals independent of the input perturbations, as illustrated in Fig. 2(a). Thus, the output power of the POL converter is constant and in turn the input power is almost constant. It is assumed that the output power of the POL converter is equal to the input power $P_i = P_o$ (hereinafter referred as P_{CPL}).



(a)



(b)

Fig. 2. (a) Block diagram of a POL converter and its input/output voltages and currents; b) CPL characteristic curve of the POL buck converter.

Therefore, POL buck converter behaves as a CPL, the control action reduces the input current if the input voltage increases and vice versa, thus, the product of the input current and input voltage is always constant (Lucas et al., 2019a; Mosskull, 2017; Tahim et al., 2015).

Fig. 3 shows a simplified DC cascaded converter system, i.e., an energy source (v_i) provides DC power through a DAB DC-DC converter, feeding a CPL.

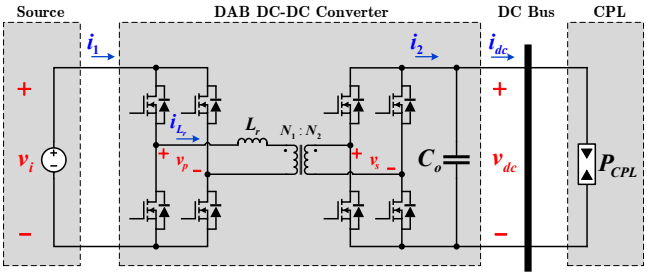


Fig. 3. Simplified DC cascaded converter system.

2.1 Constant Power Load

The voltage-current characteristics of an ideal CPL is given by

$$i_{CPL} = \frac{P_{CPL}}{v_{CPL}} \tag{1}$$

where P_{CPL} is the power of CPL, i_{CPL} and v_{CPL} are the instantaneous values of input current and voltage of the CPL.

There are two major differences between an ideal CPL and a POL buck converter. The first one occurs when the input voltage (v_{dc}) is less or equal than the voltage threshold (V_{th}), which is the designed output voltage v_o of the buck converter with control loop. At this situation, the controller saturates the duty cycle, causing the switching component to remain closed, consequently, the POL converter becomes a resistive load, losing its CPL characteristic, dividing the equivalent system in two regions as illustrated in Fig. 2(b). Therefore, the voltage-current characteristics of a POL buck converter is represented mathematically as as a piecewise function (2) (Tahim et al., 2015).

$$i_{CPL}(v_{dc}) = \begin{cases} \frac{P_{CPL}}{v_{dc}}, & \text{if} \quad v_{dc} > V_{th} \\ \frac{P_{CPL}}{V_{th}^2} v_{dc}, & \text{if} \quad v_{dc} \leq V_{th} \end{cases} \tag{2}$$

The second difference occurs at high frequencies. Ideal CPL respond equally to every frequency, whereas the POL buck converter are only able to respond to frequencies within the closed-loop bandwidth, consequently, the POL buck converter bandwidth must be sufficiently high to

make the consumed power independent of the intermediate DC bus voltage variation (Lucas et al., 2019c; Tahim et al., 2015).

The POL buck converter with the values of the parameters designed (cf. Table 1) acts as a CPL, such characteristic reflects at the input terminal a negative incremental resistance, which tends to destabilize the system (Lucas et al., 2019a,c). The operating point P_{CPL} of the POL buck converter is shown in Fig. 2(b). This confirms that the POL buck converter is operating in the constant power zone (cf. Fig. 2(b)).

2.2 DAB converter modelling with CPL

Phase shift modulation (PSM) is applied to operate the two bridges with a phase shift φ, which enables power transfer from the leading bridge to lagging bridge.

Since current i_2 and output voltage v_{dc} have largely average DC components, State Space Averaging (SSA) is applicable at the output terminal of the DAB. Writing the SSA equations from the Kirchhoff Current Law (KCL) at the output terminal of the DAB,

$$C_o \frac{d\left\langle v_{dc}(t)\right\rangle_{T_s}}{dt} = \left\langle i_2(t)\right\rangle_{T_s} - \left\langle i_{CPL}(t)\right\rangle_{T_s} \tag{3}$$

Power flow $\left\langle p(t)\right\rangle_{T_s}$ from the leading to lagging bridge can then be expressed as (Doncker et al., 1991):

$$\left\langle p(t)\right\rangle_{T_s} = \frac{N_1}{N_2}\frac{\left\langle v_i(t)\right\rangle_{T_s}\left\langle v_{dc}(t)\right\rangle_{T_s}}{2\pi f_{sw} L_r}\varphi\left(1-\frac{|\varphi|}{\pi}\right) \tag{4}$$

where f_{sw} is the switching frequency, $T_s = \frac{1}{f_{sw}}$ is the switching period, $\left\langle v_i(t)\right\rangle_{T_s}$ is the average value of v_i in a switching period, and $\left\langle v_{dc}(t)\right\rangle_{T_s}$ is the average value of v_{dc} in a switching period.

This model does not consider winding power losses and the power transferred through higher order odd harmonics. From the power balance equation, the secondary side DC current is given by the following equation:

$$\left\langle p(t)\right\rangle_{T_s} = \left\langle i_2(t)\right\rangle_{T_s}\left\langle v_{dc}(t)\right\rangle_{T_s}$$

$$\Rightarrow \left\langle i_2(t)\right\rangle_{T_s} = \frac{N_1}{N_2}\frac{\left\langle v_i(t)\right\rangle_{T_s}}{2\pi f_{sw} L_r}\varphi\left(1-\frac{|\varphi|}{\pi}\right) \tag{5}$$

To simplify analysis, let's define

$$\omega_{sw} = 2\pi f_{sw} \;\;,\;\; g_m = \frac{N_1}{N_2}\frac{1}{\pi\omega_{sw}L_r} \tag{6}$$

Substituting (2), (6) and (5) into (3), and assuming that $\varphi > 0$.

$$C_o \frac{d\left\langle v_{dc}(t)\right\rangle_{T_s}}{dt} = g_m\left\langle v_i(t)\right\rangle_{T_s}\varphi\left(\pi-\varphi\right) - \frac{P_{CPL}}{\left\langle v_{dc}(t)\right\rangle_{T_s}} \tag{7}$$

The control objective is that the DC bus voltage (v_{dc}) remains regulated even under large disturbances.

Since CPL introduces nonlinearity into system, conventional linear controllers are not sufficient to mitigate oscillations effects and ensure system stability under large signal disturbances.

3. PROPOSED CONTROL METHODOLOGY

The design procedure of the proposed controller is illustrated in this section. First, the CPL linearization is performed to overcome the non-linearity introduced by a CPL. Second, the non-linear equation (7) is transformed into a linear equation using FLC and the the CPL linearization. Finally, the robust controller design is introduced. Fig. 4 illustrates the proposed control block diagram for DAB converter feeding a CPL.

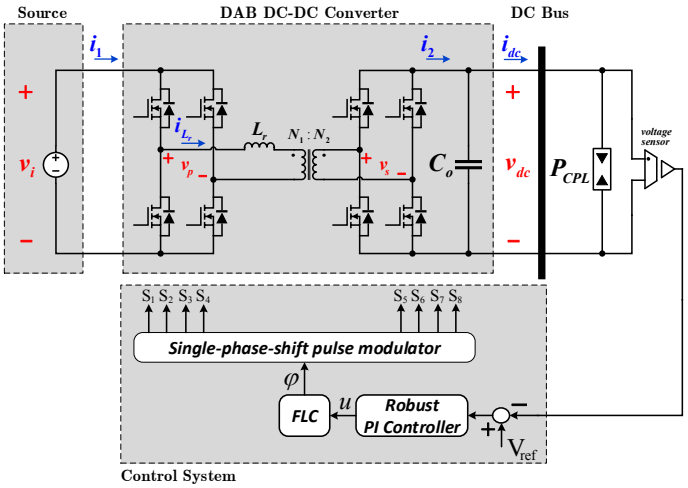


Fig. 4. Proposed Block diagram of the SPS control for DAB converter feeding a CPL.

3.1 CPL Linearization

Since the ideal CPL model is nonlinear, it is common practice to linearize it in a voltage operating point V_{dc}. Note that V_{dc} and P_{CPL} represent the dc value, i.e., the operating points. (Tahim et al., 2015).

$$i_{CPL} \approx 2\frac{P_{CPL}}{V_{dc}} - \frac{P_{CPL}}{V_{dc}^2}v_{dc} \;,\; R_{CPL} = -\frac{V_{dc}^2}{P_{CPL}} \tag{8}$$

The linearization of CPL yields the the following nonlinear equation (9) where, the CPL is linearized around the operating point.

$$C_o \frac{d\left\langle v_{dc}(t)\right\rangle_{T_s}}{dt} = g_m\left\langle v_i(t)\right\rangle_{T_s}\varphi\left(\pi-\varphi\right) - \frac{1}{R_{CPL}}\left\langle v_{dc}(t)\right\rangle_{T_s} \tag{9}$$

3.2 Feedback Linearization Control

The average model for the DAB converter with Linearized CPL (9) is nonlinear continuous-time equation due to the cross-product between phase-shift (φ) and the square of φ with the averaged input voltage of v_i. Note that the non-linearity introduced by the CPL $\left(P_{CPL}/\left\langle v_{dc}(t)\right\rangle_{T_s}\right)$ is not taking into account for the feedback linearization controller design.

The voltage control loop is designed based on the input/output FLC technique, whose objective is to provide a linear model of the system, overcoming the non-linearity (9).

Considering the dynamic equation (9) that represents the variation of average value of v_{dc} where $\left\langle v_{dc}(t)\right\rangle_{T_s}$ is the

system output and φ is the control signal, let $u(t)$ be a the auxiliary input variable to describe a new linear relationship (11) that represents the dynamics of the output voltage v_{dc}. Note that $\langle v_i(t)\rangle_{T_s} = V_i$

$$u(t) = V_i\varphi\left(\pi - \varphi\right) \tag{10}$$

$$C_o\frac{d\left\langle v_{dc}(t)\right\rangle_{T_s}}{dt} = g_m u(t) - \frac{1}{R_{CPL}}\left\langle v_{dc}(t)\right\rangle_{T_s} \tag{11}$$

Hence, the small-signal control-to-output transfer function of the DAB converter with FLC is

$$G_{vd}(s) = \frac{v_{dc}(s)}{u(s)} = \frac{g_m}{C_o}\left(\frac{1}{s + \frac{1}{C_o R_{CPL}}}\right) \tag{12}$$

In order to meet the closed-loop performance requirements, a linear controller may be designed based on (12).

3.3 Robust Control Design

The design procedure of the voltage controller is performed by using a voltage PI controller (13), which is adopted to regulate the output voltage v_{dc}.

$$C_1(s) = \frac{K_p s + K_i}{s} \tag{13}$$

The controller is designed according to Lucas et al. (2019c), which leads to a set of linear inequality constraints. This control technique is successfully employed in Lucas et al. (2019b) to control a DAB converter under parametric uncertainties. To design the controller, a region of uncertainty, defined by $[P_o^{\min}, P_o^{\max}]$, is previously defined. Thus, the uncertainties build a box region in the plant parameters, as a result, the plant-model (12) becomes in a interval plant (13).

$$G_{vd}(s) = \frac{g_m}{C_o}\left(\frac{1}{s - \frac{\Delta P_o}{C_o V_{dc}^2}}\right) = \frac{g_m}{C_o}\left(\frac{1}{s - \frac{[P_o^{\min},\ P_o^{\max}]}{C_o V_{dc}^2}}\right) \tag{14}$$

The interval characteristic polynomial of the closed-loop system is by using the controller (13) and the interval plant (14) parameters.

$$[\Delta(s)] = s^2 + \left(\frac{g_m}{C_o}K_p - \frac{\left[P_o^{\min},\ P_o^{\max}\right]}{C_o V_{dc}^2}\right)s + \frac{g_m}{C_o}K_i \tag{15}$$

Assuming that the desired dynamic of closed-loop system is represented by

$$\Delta_d(s) = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{16}$$

The region defined by the closed-loop interval characteristic polynomial (15) must be inside the region determined by the desired performance polynomial (16). Thereby, a desired region is defined as follows:

$$\Phi(s) = \left[\Delta_d^{\min}, \Delta_d^{\max}\right] = s^2 + [\ \phi_1\ ]s + [\ \phi_o\ ] \tag{17}$$

where $[\ \phi_1\ ] = [\phi_1^{\min}, \phi_1^{\max}]$ and $[\ \phi_o\ ] = [\phi_o^{\min}, \phi_o^{\max}]$

In order to tune the controller, the closed-loop parameters obtained (15) are compared with the parameters of the interval closed-loop desired polynomial ($[\Delta(s)] = \Phi(s)$). This problem can be written in its matrix representation (18).

$$\begin{bmatrix} \frac{g_m}{C_o} & 0 \\ 0 & \frac{g_m}{C_o} \end{bmatrix}\begin{bmatrix} K_p \\ \\ K_i \end{bmatrix} = \begin{bmatrix} [\,\phi_1\,] + \frac{\Delta P_o}{C_o V_{dc}^2} \\ \\ [\,\phi_1\,] \end{bmatrix} \tag{18}$$

Therefore, according to Lucas et al. (2019c), it is possible to formulate a linear inequalities set (19), which restricted the controller and desired polynomial coefficients in the predefined intervals.

$$\begin{bmatrix} \phi_1^{\min} + \frac{\Delta P_o}{C_o V_{dc}^2} \\ \\ \phi_o^{\min} \end{bmatrix} \leq \begin{bmatrix} \frac{g_m}{C_o} & 0 \\ 0 & \frac{g_m}{C_o} \end{bmatrix}\begin{bmatrix} K_p \\ \\ K_i \end{bmatrix} \leq \begin{bmatrix} \phi_1^{\max} + \frac{\Delta P_o}{C_o V_{dc}^2} \\ \\ \phi_o^{\max} \end{bmatrix} \tag{19}$$

Thus,

$$B(\phi^{\min}) \leq AX \leq B(\phi^{\max}) \tag{20}$$

The robust design problem is summarized in the choice of $X = [\,K_p \quad K_i\,]^T$ (if possible) to satisfy the set of inequality (20). The solution of this problem can be idealized, as a solution to a linear programming problem. Therefore, this problem (20) can be rewritten as a problem of local minimization, subject to restrictions according to Lucas et al. (2019a).

$$\begin{aligned} &X_a = \arg\left(\min f(X_a)\right) \\ &s.t. \begin{bmatrix} A_a \\ -A_a \end{bmatrix} X_a \leq \begin{bmatrix} B(\phi^+) \\ -B(\phi^-) \\ 0 \end{bmatrix} \end{aligned} \tag{21}$$

with

$$X_a = \begin{bmatrix} X \\ R \end{bmatrix},\ A_a = \begin{bmatrix} A & \|a\|_2 \\ -A & \|a\|_2 \\ 0_{1\times 2} & -1 \end{bmatrix} \tag{22}$$

where, $\|a\|_2$ is the euclidean norm of coefficients of A; the cost function is defined as the sum of controller gains within the radio R and the parameter vector X_a contains the controller gains and the radio of the largest ball of Chebyshev Theorem.

Then, the feasible solution is used to set the control structure (13). In order to obtain the discrete equivalent of the designed controller, the Tustin method is used to perform the discrete approximation, using a sampling rate of $T_s = 1/f_{sw}$.

Finally, according to (10), the value of the control φ actually sent to the SPS pulse modulator is determined by,

$$\varphi = \frac{\pi - \sqrt{\pi^2 - \frac{4u}{V_i}}}{2} \tag{23}$$

where, $\pi^2 - \frac{4u(t)}{V_i} > 0$, and the solution for φ is the negative root since φ is defined in the control design to operate from 0 to $\frac{\pi}{2}$.

4. CONTROLLERS DESIGN

This paper analyzes the control performance of the proposed controller (Robust FLC) in comparison with a classical controller, based on pole-placement, a robust controller, based on Lucas et al. (2019b), and a feedback

linearization controller. All controllers regulate the output of the DAB converter under CPL power variation and input voltage variation. All controller gains are obtained by the authors according to the procedure described below.

In order to design the controllers, the following (nominal) requirements are chosen to regulate the output of the DAB converter: settling time $t_{set} \leq 30$ ms and damping factor $\xi \geq 0.69$, defining desired dynamic of the closed-loop system $\Delta_d(s)$ (15).

The desired performance region $\Phi(s)$ (16) is obtained by varying the nominal closed-loop desired poles as follows,

$$\begin{aligned} t_{set} &= 100ms \pm 25\% \\ \xi &= 0.69 \pm 25\% \end{aligned} \tag{24}$$

By using the proposed control technique, the robust feedback linearization controller is designed. The feedback linearization controller is based on classical pole-placement control using the nominal model with FLC (11) to meet the nominal performance requirements.

The classical controller is based on classical pole-placement control using a small-signal model $G_2(s)$ by linearizing the nonlinear equation (7).

$$G_2(s) = \frac{N_1}{N_2} \frac{(\pi - 2D_\varphi)}{\pi \omega_{sw} L_r C_o} \left(\frac{V_i}{s - \frac{P_o}{C_o V_{dc}^2}} \right) \tag{25}$$

By introducing the box region of uncertainties (cf. Table 1) into (24) and using desired performance region $\Phi(s)$ (16), the robust controller is designed.

It is important to mention that for the cases of classical and robust controller, i.e., the controllers without FLC, the output of these controller is the phase-shift φ that controls the SPS modulator.

On the other hand, to regulate of the output of the buck converter (P_o), the following requirements are considered: settling time $t_{set_2} \leq 10$ ms and damping factor $\xi_2 \geq 0.9$.

Table 2 summarizes each controller gains for the designed controllers.

Table 2. Values of parameters for the designed controllers.

Controller Gains	k_p	k_i	k_d
DAB Converter			
Classical Control	0.00198	0.5039	-
Robust Control	0.00451	0.6372	-
Feedback Linearization Control	8.74518	844.25	-
Robust FLC	7.65409	1595.1	-
POL Buck Converter			
Classical Control	$1.729e^{5}$	0.0353	$1.756e^{8}$

5. ASSESSMENT OF RESULTS

The experiments described below are performed using MATLAB/Simulink. The aim is to check the oscillations effects in the intermediate DC bus voltage (v_{dc}) caused by CPL power variation (P_{CPL}) and input voltage variation (v_i).

5.1 CPL Power Variation

This experiment evaluates the closed-loop performance under CPL power variation. After the cascaded converter system reaches its steady state (cf. Table 1), the system is subjected to a CPL power variation from 2000W to 3000W (ΔP_{o1}) at time t = 0.4s. Then, at time t = 0.7s, another variation of CPL power is performed from 3000W to 1000W (ΔP_{o2}). Finally, the CPL power returns to the value of 3000W at t = 1.0s (ΔP_{o3}), as shown in Fig. 5.

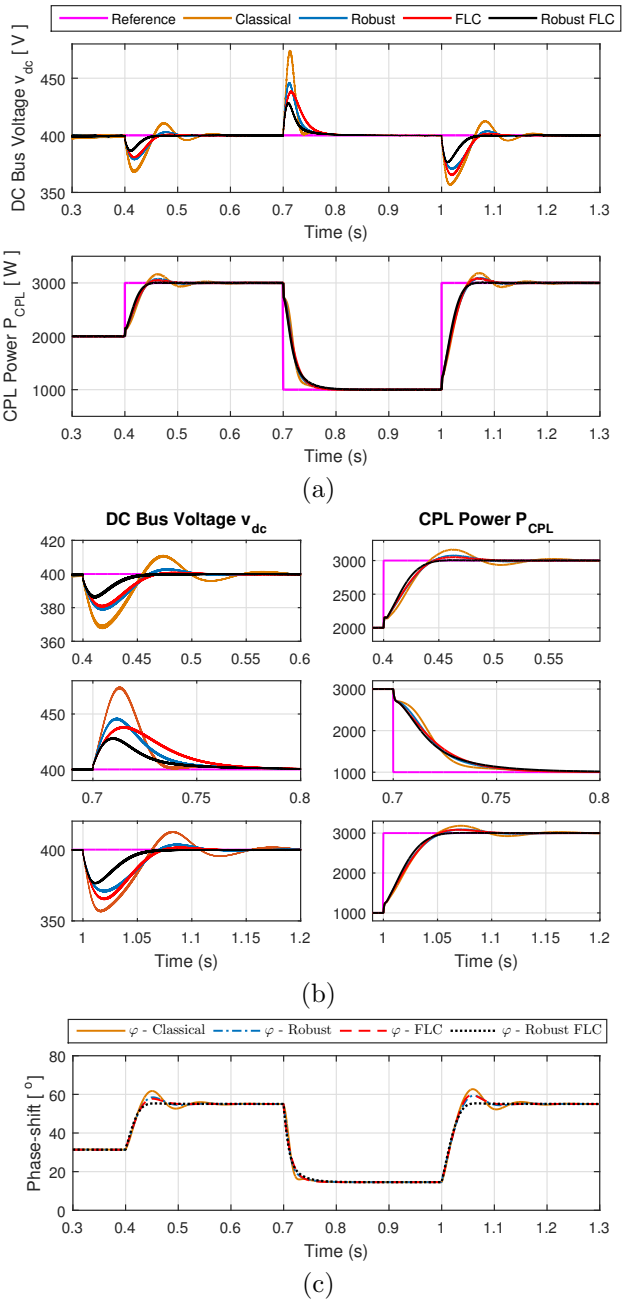


Fig. 5. CPL power variation test. (a) System performance under CPL power variation. (b) Zoomed area near of each variation. (c) Phase-Shift control φ.

The simulated results demonstrate that all controllers of source converter can compensate oscillations into the DC bus voltage (v_{dc}) and ensure system stability under CPL power variations. However, the proposed controller

more effectively compensates the oscillations caused by CPL power variation, reducing the oscillation amplitude in comparison with other control approaches with faster transient. Therefore, the impact of CPL power variations is reduced when the proposed controller is used, as shown by the ISE and ITAE performance indices in Table 3, ratifying the robustness of the proposed methodology.

Table 3. Performance Indices for CPL power variation test.

CPL power Variation	ΔP_{o1}	ΔP_{o2}	ΔP_{o3}
	ISE Index (e^7)		
Classical Control	26.526	42.285	50.608
Robust Control	10.208	20.209	24.019
FLC	9.166	18.445	30.503
Robust FLC	3.178	7.980	10.511
	ITAE Index (e^6)		
Classical Control	6.407	6.292	19.797
Robust Control	3.317	5.035	12.349
FLC	3.125	5.437	12.919
Robust FLC	1.729	3.369	6.987

5.2 Input Voltage Variation

This experiment evaluates the closed-loop performance under input voltage variation. When the cascaded converter system is operating in its steady state (400V and 2000W), the system is subjected to a input voltage variation from 800 V to 900 V (ΔV_{i1}) at time t = 0.4s. Then, another input voltage variation is performed (ΔV_{i2}), returning to its initial condition ($V_i = 800V$) at time t = 0.8s.

Fig. 6 shows the simulated results of closed-loop system performance for input voltage variation.

The proposed controller (Robust FLC) and the feedback linearization controller (FLC) outperforms the other controllers. For the robust FLC and FLC, the transient responses remain constant (cf. Fig. 6(a)), independently on the operating point of input voltage (v_i) because, for the feedback linearization cases, the controller design is based on the linearization of the nonlinear averaged equations (9) by means of nonlinear control laws. For that reason, the phase-shift control value (22) for the SPS modulator is instantly found when a variation in input voltage occurs (cf. Fig. 6 (c)).

Table 4 shows the ISE and ITAE performance indices, which ratify the affirmation above mentioned.

Table 4. Performance Indices for input voltage variation test.

CPL power Variation	ΔV_{o1}	ΔV_{o2}	ΔV_{o1}	ΔV_{o2}
	ISE Index (e^7)		ITAE Index (e^6)	
Classical Control	2.484	13.286	2.075	6.389
Robust Control	1.043	5.5451	1.602	4.075
FLC	0.089	0.0181	0.995	0.898
Robust FLC	0.092	0.0184	1.055	0.906

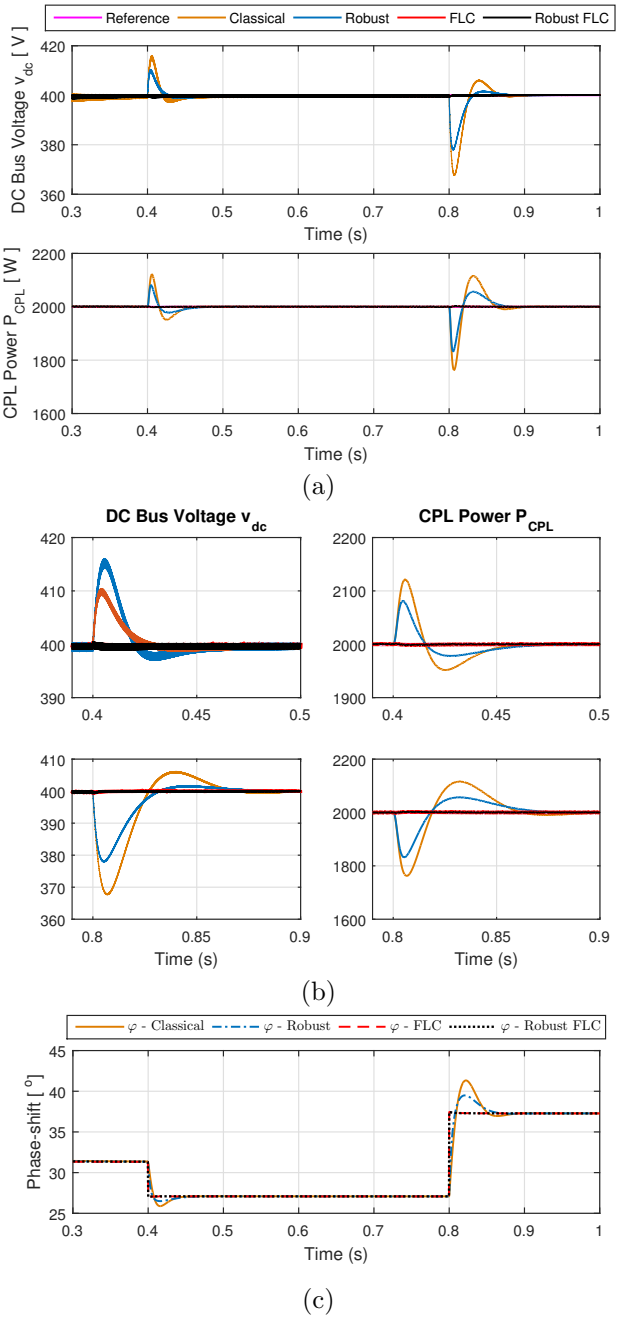


Fig. 6. Input voltage variation test. (a) System performance under CPL power variation. (b) Zoomed area near of each variation. (c) Phase-Shift control φ.

6. CONCLUSION

This paper proposes a robust feedback linearization control approach for designing fixed order nonlinear robust controller, in order to minimize oscillation effects caused by constant power load in a cascaded converter system, ensuring robust stability and robust performance for an entire predefined uncertainty region. The proposed design method based on the combination of FLC and robust linear design can be extended to other system applications modelled by nonlinear equations. The proposed controller performance is compared with a classical controller, a robust controller, and feedback linearization controller.

The simulated results show that the proposed control approach provides a better performance, compensating the oscillations introduced by CPL more effectively with reduced oscillation amplitude and faster transient response. In addition, the proposed control approach ensures a transient performance independent of the operating point of the input voltage (v_i). The performance indicators comparison confirm the robustness of the proposed controller.

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