A Modified PFC Rectifier Based EV Charger Employing CC/CV Mode of Charging \star

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Abstract: Automobile industry has displayed an inclination towards Electric Vehicles (EVs). However, EVs charging throws inevitable challenges due to inclusion of non-linear charger circuitry. The conventionally utilized AC-DC rectification in charger poses ruinous effects to Grid and EV structure in the form of harmonics interference and obnoxious spikes in current. Thus, repercussions of elevated THD can be witnessed in poor efficiency and deterioration of EV charger. Furthermore, harmonics in input inductor current produce harmonics in rectifier's output voltage. This can lead to DC link voltage fluctuation and adversely affect DC/DC converter functioning. Henceforth, a Power Factor Correction (PFC) rectifier based charger has been proposed that eliminates unwanted harmonics from input current and reduces THD. Moreover, harmonics in rectifier's output voltage are reduced and constant DC link voltage is obtained. Sinusoidal input current is maintained through Critical Conduction Mode (CrCM) and hysteresis current control application. These are achieved using inner current and outer voltage control loop method. The former produces sinusoidal current wave in phase with input voltage to improve power factor. Whereas, latter helps in achieving constant DC link voltage. Hence, THD factor of 1.30% and power factor of 0.9998 are recorded. In addition, model inculcates CC/CV charging algorithm to control overcharging of battery. Here, battery charges at Constant Current (CC) initially. Once, maximum voltage is reached, charging occurs at Constant Voltage (CV). It is governed by two isolated PI controllers. The collaborated work of PFC and CC/CV helps in recording model's efficiency of 96.8%. Furthermore, a 2 kW charger prototype is analysed using real time simulation and validated through Hardware-in-loop (HIL) in OPAL-RT.

Keywords: CC/CV, CrCM technique, Hysteresis current control, OPAL-RT, PFC rectifier, Power factor improvement, THD reduction.

1. INTRODUCTION

Recent years have witnessed massive decline in fossil fuels. Therefore, an inclination towards battery operated vehicles is noticeable. However, EV demands a charger which provides high power factor, low THD injection, good efficiency and controlled charging of the battery according to The rudimentary charging strategy opts an AC-DC approach. But, non linear nature of circuitry injects harmonic in Grid and THD factor is elevated.

Evidently, battery charging is segregated into two halves. The first stage is responsible for generating stable DC link voltage, minimum THD and less harmonic injection into Grid according to Hence, a special type of rectifier called PFC rectifier can be utilized to perform these functions. Its objective is to generate a sinusoidal input inductor current waveform in phase with input voltage. Hence, improvement in power factor can be observed and THD can be reduced.

Researchers have worked upon different PFC topologies. To make compact circuit, Hsing-Fu Liu and Lon-Kou Chang (2005) proposed reduction in inductor size by including an extra winding in transformer's primary of flyback converter. However, its use increased the size of rectifier circuit. It operated in pseudo continuous conduction mode (PCCM) providing fast transient response but failed to provide low THD. Also, a discontinuous conduction mode based PFC rectifier had been analysed by Lee and Chae (2014), but it involved numerous switches making the system bulky. Hence, according to Yang et al. (2010), CrCM technique was preferable due to its easy implementation and zero requirement of pseudo limits. Also, the successful execution of PFC is possible when input inductor current and input voltage are in phase with each other

Apparently, among a number of PFC topologies, the boost topology was estimated to perform more efficiently, offering no inherited cross over distortions in the input current, smooth control and less THD in output Wang et al. (2013). Hence, present investigation aims at proposing a model which is a combination of diode bridge coupled with boost

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converter. O'Sullivan et al. (2000), discussed about its implementation using divider and multiplier circuits, peak and zero identification of voltage. The necessary calculations of L and C as provided in by Hart (2011) proved relevant.

The second stage is responsible for ensuring controlled charging of battery and eliminating chances of overcharging. Various algorithms were devised such as Constant-Current (CC) and Constant-Voltage (CV). CC method showcases the ability to quickly charge the battery but it poses a problem of overcharging The CV approach eliminates the problem of overcharging but increases the charging time. Therefore, Constant-Current Constant-Voltage (CC/CV) has been utilised in proposed model.

It can be deduced from previous research work that limited focus has been put on incorporation of both PFC rectifier and CC/CV charging algorithm in EV charger. proposed a PFC charger that used probabalistic fuzzy neural network (PFNN) for implementing CC/CV algorithm. Though, the authors were able to establish smooth transition between CC and CV modes but the input current THD was recorded at 4.1%. Later, a full bridge LLC based PEV charger was presented by Wang et al. (2014) and the THD was dropped down to a value of 3.6%. Shi et al. (2017) reduced the THD to as low as 2.72%. O'Sullivan et al. (2000) designed charger implementing resonant power conversion technique but, the overall efficiency obtained was 70%.

However, all the above mentioned designs employed numerous switches and diodes which resulted in several losses and a bulky charger. Moreover, this model has achieved a THD of 1.30% with an efficiency of 96.8%.

1.1 Motivation

A lot of research has been contributed towards EV charging. Some of the key features can be referred as CC/CV charging algorithm and PFC rectification. Though numerous researches had been focussed on PFC rectification and CC/CV charging, few is dedicated to inclusion of CrCM technique of correcting power factor. Moreover, the researchers were able to reduce the THD upto 2.72% with the attained efficiency of 93.5%. Hence, this motivated authors to amalgamate controlled circuitry of PFC Rectifier and CC/CV mode of charging. This not only provides high power factor and efficiency but attains less THD and harmonic injection.

1.2 Contributions

The major contributions of this paper are listed as follows.

- Detailed modelling, design and operational analysis of PFC rectifier is done to accomplish 0.9998 power factor, 1.30% THD and efficiency of 96.8% by optimal selection of control strategy and components.
- Controlled charging of battery is obtained through implementation of CC/CV algorithm.
- Investigation of system is carried out through Matlab Simulink and experimental validation is done through hardware-in-loop (HIL) in OPAL-RT.

1.3 Organisation

The further outline of paper can be summarised in following sections. Section II discusses the framework of system. Section III formulates the problem. Section IV displays analysis of results and section V finally provides conclusion of paper.

2. SYSTEM FRAMEWORK

The proposed model is a PFC based EV charger achieved through realisation of CrCM based Boost PFC Rectifier that obeys zero current switching (ZCS). As a result, minimal switching losses are observed during turn on. It can be observed from Fig. 1 that block diagram of PFC based EV charger charges the battery in two stages. The first stage is the Boost PFC Rectifier stage whereas, the second stage is of Controlled Battery Charging using DC/DC buck converter. Considering first stage of Fig. 1, the objective is to eliminate harmonics in input inductor current, improve power factor and generate constant DC link voltage. Its detailed working mechanism can be found as below.

2.1 Working of Boost PFC Rectifier stage

Initially, the source voltage V_s is converted to a pulsating DC voltage V_i via diode bridge rectifier as depicted in Fig. 1. This V_i acts as input for the boost converter of PFC rectifier. Boost converter adds a resistive load to the non linear rectifier's circuitry. Therefore, it aims to produce sinusoidal input inductor current in phase with the input voltage. Its control strategy is sectioned into two parts namely, outer voltage and inner current control loop. The outer voltage control loop is responsible for generating constant DC link voltage at the output of boost converter. Whereas, the inner current control loop is responsible for generating sinusoidal input current in phase with the input voltage.

The outer voltage control loop involves voltage sensing circuit which generates constant DC link voltage across boost capacitor, $C_{\rm bst}$. Here, a reference voltage $V_{\rm ref}$ is set which is compared with the voltage $V_{\rm dc(link)}$ sensed from $C_{\rm bst}$. Meanwhile, to generate sinusoidal input inductor current, inner current control loop begins its operation. A programmed current signal $I_{\rm m}^*$ is produced as shown in Fig. 1 as a replica of input voltage waveform. This when multiplied with $V_{\rm p}$, generates reference current denoted as $I_{\rm L}^*$. The current signal from inductor, $I_{\rm L}^0$ is sensed and compared with reference value.

The model follows CrCM operation to achieve an input inductor current sinusoidal and in phase with input voltage. Under this mechanism, the switch is turned on at zero current crossing and turned off when it touches peak. Furthermore, the error obtained is compared with the limit band of hysteresis controller. As a result, output is used to drive the switch of boost converter.

2.2 Working of Controlled Battery Charging stage

The constant voltage at the DC link, V_{dc} behaves as input for buck converter. Initially, the charging of battery is



Fig. 1. Block diagram of proposed charger

carried out in CC mode. Here, a current reference, $I'_{\rm ref}$ is set and compared with current sensed from battery, $I_{\rm bat}$. Since, during charging the value of sensed current will vary, a Constant Current (CC) mode Controller is employed to tune error according to reference value. This controller generates pulses to drive buck converter's switch during CC mode.

However, during this phenomenon, the battery's SoC rises quickly and charging voltage gradually increases. The increasing battery voltage, V_{bat} is compared with reference voltage, V'_{ref} . Once, V_{bat} reaches V'_{ref} , it is held constant. At that instant, the threshold switch makes transition from CC to CV mode. The error is tuned via Constant Voltage (CV) mode Controller and pulses are generated to switch.

3. PROBLEM FORMULATION

This section focusses on modelling details of proposed EV charger. Here, emphasis is laid on developing simple and fast control strategy for proposed model. The specifications are mentioned in Table. 1. The mathematical and operational analysis of Boost PFC rectifier stage and Controlled battery charging stage are carried out separately as below.

3.1 Boost PFC Rectifier

The controlling and modelling equations of PFC rectifier are discussed below.

Controlling of Boost PFC Rectifier Programmed current signal, $I_{\rm m}^*$ is obtained as suggested in the following equation. It is a signal having waveshape of input voltage but, of unit magnitude and pulsating DC nature.

$$I_m^* = \frac{|V_s|}{V_{s(max)}} = \frac{|V_{s(max)}sinwt|}{V_{s(max)}}$$
(1)

A constant DC link voltage is generated using an outer voltage control loop. It is done by comparing $V_{\rm ref}$ as observed from Fig. 1 with $V_{\rm dc(link)}$. The error generated denoted by $V_{\rm e}(t)$ after comparison can be analysed using following equation.

$$V_e(t) = V_{ref} - V_{dc(link)} \tag{2}$$

Now, this error behaves as input to voltage controller and is reduced by implementing PI controller as mentioned in (3). Here, the output received is referred as peak voltage, $V_{\rm P}$.

$$V_p = K_{p1} * V_e(t) + \frac{K_{p1}}{T_i} * \int V_e(t)dt$$
(3)

where, $K_{\rm p}$ is the proportional constant and $\rm K_p/T_i$ is the integral constant. To realise a sinusoidal input current waveform, a reference current signal is generated through inner current control loop. Thus, $V_{\rm p}$ and $I_{\rm m}^*$ as obtained using (3) and (1) respectively, are used to generate $I_{\rm L}^*$ according to (4). The peak voltage waveform when multiplied with a unit magnitude signal produces an output of peak voltage magnitude. Thus, $I_{\rm L}^*$ received is pulsating DC.

$$I_L^* = V_p * I_m^* \tag{4}$$

Furthermore, current signal sensed from the input inductor is compared with the reference current. Henceforth, $I_{\rm L}^*$ as obtained from (4) is compared with $I_{\rm L}^0$ for error detection as in (5). The output drives switch of boost converter whose duty ratio can be expressed as,

$$I_e(t) = I_L^* - I_L^0$$
(5)

$$V_{dc(link)} = \frac{V_i}{1 - D} \tag{6}$$

Modelling of Boost PFC Rectifier It includes calculation of inductance 'L' and capacitance 'C' parameters. The mathematical value of $L_{\rm bst}$ lies between $L_{\rm bst(min)}$ and $L_{\rm bst(max)}$ which are evaluated as below.

$$L_{bst(min)} = \frac{V_i * D}{2 * f_s * I_{L(avg)}}$$
(7)

$$L_{bst(max)} = \frac{V_i * D}{f_s * \Delta I_L} \tag{8}$$

where, $f_{\rm s}$ is switching frequency, $\triangle I_{\rm L}$ represents the permissible current ripple and $I_{\rm L(avg)}$ denotes average inductor current. The relation between $\triangle I_{\rm L}$ and $I_{\rm L(avg)}$ can be found in the following equation.

$$\frac{\Delta I_L}{2} = I_{L(avg)} \tag{9}$$

$$I_{L(avg)} = 5\% * I_{source} \tag{10}$$

The capacitance 'C' of the boost converter can be found by using the equation as mentioned under. Here, 'R' is the load resistance

$$C = \frac{V_{dc(link)} * D}{\triangle V * R * f_s} \tag{11}$$

3.2 Controlled Battery Charging

Battery is charged using CC/CV mode of charging algorithm. The detailed explanation of controlling and modelling of this stage can be found underneath.

Controlling of Battery charging In CC mode, the current flowing to the battery has to be kept constant. Thus, I_{bat} is compared with the reference current I'_{ref} to generate error $I_{\text{e(cc)}}(t)$ to CC controller. This is represented using the following equation.

$$I_{e(cc)}(t) = I_{bat} - I'_{ref} \tag{12}$$

The duty cycle $D_{\rm CC}$ will be generated via condition switch till $I_{\rm bat}$ and $I'_{\rm ref}$ are equal. It verifies the condition of incrementing voltage touching pre-set voltage. If the condition is false, $D_{\rm CC}$ will be passed to buck converter switch. It is obtained as,

$$D_{CC} = K_{p(CC)} * I_{e(CC)}(t) + \frac{K_{p(CC)}}{T_i} * \int I_{e(CC)}(t) dt (13)$$

Once, the voltage sensed from the battery V_{bat} becomes equal to the reference voltage V'_{ref} , the condition in the 'condition switch' becomes true. As a result, D_{CV} will be generated to the buck converter switch. The equation is obtained as under.

$$V_{e(CV)}(t) = V_{bat} - V'_{ref} \tag{14}$$

$$D_{CV} = K_{p(CV)} * V_{e(CV)}(t) + \frac{K_{p(CV)}}{T_i} * \int I_{e(CV)}(t) dt (15)$$

Modelling of Buck Converter $V_{dc(link)}$ is stepped down to a battery compatible value. The modeling of inductance L_{bck} and capcitance C_{bck} can be done using the following equations.

$$L_{bck} = \frac{(V_{in} - V_0) * D}{\triangle I_L * f_s} \tag{16}$$

$$C_{bck} = \frac{\triangle I_L}{8 * f_s * \triangle V_0} \tag{17}$$

The efficiency, η , of proposed EV charger can be evaluated as mentioned in below equation. Since, V_{bat} and I_{bat} vary, the output power may vary hence, affecting input power. However, at any point of time, the ratio of P_{out} and P_{in} remains constant.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{bat} * I_{bat}}{V_s * I_s * \cos(\alpha)}$$
(18)

It can be deduced that the implementation of proposed model relies on proper execution and synchronisation of control strategy and appropriate selection of the components.

4. RESULTS AND DISCUSSION

This section draws comparison between OPAL-RT simulated and hardware-in-loop (HIL) results according to the model specifications mentioned in Table. 1.A 2 kWh EV battery charger is simulated and experimentally analyzed for the desired outputs. The detailed discussion is described in the sections following.

Table 1. Design parameters of proposed EV charger

Symbol	Quantity or device	Spec.
V_{ref}	Reference Voltage	300 V
L _{bst}	Boost Inductor	40.738 mH
C_{bst}	Boost Capacitor	0.03875 F
K_{p1}	Proportional Constant for stage 1	0.03
K_{i1}	Integral Constant for stage 1	0.3
LBck	Buck Inductor	0.096
C_{Bck}	Buck Capacitor	0.625 uF
f_s	Switching Frequency	5 kHz
V_{ref}'	Reference Battery Voltage	134 V
I'_{ref}	Reference Battery Current	15 A
$K_{p(CC)}$	Proportional Constant (CC) mode	10
$K_{i(CC)}$	Integral Constant (CC) mode	0.095
$K_{p(CV)}$	Proportional Constant (CV) mode	5
$K_{i(CV)}$	Integral Constant (CV) mode	0.01

4.1 Simulation Results

A Lithium - Ion EV battery of 15 Ah capacity with 120 V as the nominal voltage is charged utilizing Boost PFC rectifier and controlled battery charging. The simulated results are sectioned into two categories which are further described.

Boost PFC Rectifier stage As discussed in section II, the outer voltage control loop focuses on maintaining $V_{\rm dc(link)}$ about set $V_{\rm ref}$. It can be observed from Fig. 2 that the voltage control loop has successfully produced a constant DC link voltage of 300 V after initial transient state. It assures fast response and constant input to the buck converter. Furthermore, the inner current control



Fig. 2. DC link voltage

loop is dedicated towards waveshaping of the current and



Fig. 3. Input inductor current

removing harmonic contents in the signal. Hence, it is evident from Fig. 3 that current waveform of pulsating DC

nature is successfully obtained via accurate controlling of the current control loop. This futher aids in deduction of harmonic interference with the EV circuitry.



Fig. 4. In-phase source voltage and source current

As an outcome of harmonic minimisation, power factor of the model is improved. It can be observed from Fig. 4 that source voltage and source current are in phase with each other. The zero crossing of source voltage coincides with the zero crossing of source current. Therefore, a resistive load is achieved with the inclusion of PFC rectifier which clearly indicates high power factor. The recorded power factor was found to be equal to 0.9998.

Controlled Battery Charging stage The basic objective is to supply controlled charge to the battery by employing CC/CV mode of charging algorithm. CC mode controller works when constant current charging has to be carried out. Whereas, CV mode controller works when charge has to be provided at constant voltage.



Fig. 5. State of Charge

Before initiation of battery charging, its SOC is set at 76% as depicted in Fig. 5. Taking into consideration Fig. 6 and Fig. 7, it can be observed that charging of battery occurs at current of 15 A $(I'_{\rm ref})$ initially for approximately 90 seconds. Here, the current is held constant and the battery is charged under CC mode. Whereas, the voltage rises exponentially during that interval. To avoid over charging, it is shifted from constant current to constant voltage charging.



Fig. 6. Battery Current

Once, voltage reaches 134 V ($V'_{\rm ref}$), the charging shifts from CC to CV mode. Here, the voltage is held constant while the current starts dropping. The THD factor variation is observed during battery charging process. It can be analysed from FFT analysis of the signal that there is a drop in THD factor during charging of battery. Hence, THD factor of 1.30% was obtained with the proposed charger.



Fig. 7. Battery Voltage



Fig. 8. THD Factor in CV mode

4.2 Hardware-in-Loop results

The laboratory setup of PFC based EV charger prototype is depicted in Fig. 9. The Analog inputs such as V_{bat} and I_{bat} are sensed via voltage and current sensors and fed to the OPAL-RT. The model runs into CC or CV mode of charging according to current and voltage level of battery and generates pulses to the switch of buck converter. The digital output port of OPAL-RT is used to feed pulses to switch.

For the initial PFC rectification stage, the source voltage and source current are observed as shown in Fig. 10. The source voltage and current are sinusoidal in nature. Also, the maximum value of voltage, $V_{\rm max}$ is 15.5 V with $V_{\rm Pk-Pk}$ as 30.8 V. The maximum value of current, $C_{\rm max}$ is 11.6 A with $C_{\rm Pk-Pk}$ as 22.5 A. The realisation of nearly sinusoidal nature helps in harmonic reduction and THD factor. Therefore, the Fig. 11 shows that voltage and current are in phase with each other with zero phase angle.

Fig. 12 indicates rectified input voltage and input inductor current respectively. This clearly indicates that reduction of THD factor and harmonic interference is achieved through proposed model. It can be observed from the figure that $V_{\rm max}$ is 11.2 V whereas, $V_{\rm Pk-Pk}$ is 11.3 V. Furthermore, the maximum value of current signal, $C_{\rm max}$ is 11.3 A and its peak to peak value, $C_{\rm Pk-Pk}$ is recorded at 10.7 A.

5. CONCLUSION

A 2 kW EV charger is proposed in this paper. The boost PFC rectifier improves power factor at the grid side, removes input current harmonics and ensures constant DC link voltage at the bus capacitor. This helps in achieving good power quality. The second stage comprises of



Fig. 9. Laboratory prototype of proposed PFC based EV Charger



Fig. 10. Source voltage (CH1) and source current (CH2)



Fig. 11. In-phase source voltage (CH1) and source current (CH2)



Fig. 12. Rectified input voltage (CH3) and input inductor current (CH4) signals

controlled battery charging that charges the battery using CC/CV algorithm. The charger achieves input power factor of 0.9998, THD equal to 1.30% and 96.8% efficiency.

Moreover, the proposed scheme accomplishes higher harmonic reduction and power factor while keeping the circuit compact and efficient.

REFERENCES

Hart, D.W. (2011). Power electronics.

- Hsing-Fu Liu and Lon-Kou Chang (2005). Flexible and low cost design for a flyback ac/dc converter with harmonic current correction. *IEEE Transactions on Power Electronics*, 20(1), 17–24. doi:10.1109/TPEL.2004.839879.
- Lee, J. and Chae, H. (2014). 6.6-kw onboard charger design using dcm pfc converter with harmonic modulation technique and two-stage dc/dc converter. *IEEE Transactions on Industrial Electronics*, 61(3), 1243–1252. doi: 10.1109/TIE.2013.2262749.
- O'Sullivan, D., Willers, M., Egan, M.G., Hayes, J.G., Nguyen, P.T., and Henze, C.P. (2000). Power-factorcorrected single-stage inductive charger for electricvehicle batteries. In 2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018), volume 1, 509–516 vol.1. doi: 10.1109/PESC.2000.878914.
- Shi, C., Wang, H., Dusmez, S., and Khaligh, A. (2017). A sic-based high-efficiency isolated onboard pev charger with ultrawide dc-link voltage range. *IEEE Transactions on Industry Applications*, 53(1), 501–511. doi: 10.1109/TIA.2016.2605063.
- Wang, H., Dusmez, S., and Khaligh, A. (2013). Design considerations for a level-2 on-board pev charger based on interleaved boost pfc and llc resonant converters. In 2013 IEEE Transportation Electrification Conference and Expo (ITEC), 1–8. doi: 10.1109/ITEC.2013.6574508.
- Wang, H., Dusmez, S., and Khaligh, A. (2014). Design and analysis of a full-bridge llc-based pev charger optimized for wide battery voltage range. *IEEE Transactions on Vehicular Technology*, 63(4), 1603–1613. doi: 10.1109/TVT.2013.2288772.
- Yang, J., Zhang, J., Wu, X., Qian, Z., and Xu, M. (2010). Performance comparison between buck and boost crm pfc converter. In 2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL), 1–5. doi:10.1109/COMPEL.2010.5562437.