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A High Dynamic Range $\Delta\Sigma$ Modulator using Anti-Windup Compensated Integrators

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Abstract: This paper presents a continuous-time (CT) $\Delta\Sigma$ modulator employing an anti-windup (AW) feedback control technique to mitigate integrator overload and maintain an acceptable performance simultaneously. The proposed technique accommodates a large dynamic range and can be applied to multi-loop modulators. According to simulations, using AW augmentations, for a 50% higher dynamic range (DR), integrators do not overload and the signal-to-distortion-ratio (SNDR) drops less than 1dB from the maximum SNDR of the modulator.

Keywords: $\Delta\Sigma$ Modulator, Anti-Windup, Integrator Overloading

1. INTRODUCTION

Delta-sigma analog-to-digital converters (ADCs) have been extensively used for applications requiring a wide dynamic range (DR) such as digital audio (Wang, et al. (2016)), wireless communication (Bettini, et al. (2015)), and biomedical electronics (Yeknami, et al. (2014,2018)). A wide DR can be achieved by increasing either the number of quantization levels or the loop filter order. The latter often causes instability, while the former needs a highly linear multi-bit digital-to-analog converter (DAC). To avoid instability, single-loop high-order (> 2) modulators require intensive signal scaling by insertion of loop coefficients and/or reduction of internal signal swing (Marques, et al. (1998)), but these restrict the DR. On the other hand, cascading of stable first- or second-order modulators can build stable high-order modulators, but modulators are sensitive to non-idealities in the analog components, requiring expanded performance enhancing parameters, and thus, excessive power consumption.

Performance of single-loop high-order $\Delta\Sigma$ modulators ($\Delta\Sigma$Ms) is mainly restricted by integrator overloading. Large internal signals may overload the integrator/op-amp, particularly when the input amplitude approaches the modulator's full-scale level (i.e, the designed range limit). The quantizer then cannot follow the large internal signal effectively, which causes the signal to grow further inside the loop, leading to poor performance for the modulator. This signal limitation, caused by integrator overload, will lead to nonlinear behavior, thereby generating harmonic distortion in the output power spectrum.

Design efforts have been made in the past to overcome this issue. In Au and Leung (1997) stability is achieved by bounding the internal node voltages through insertion of local feedback loops, eventually leading to increased implementation complexity. In Zourntos and Johns (2002), the authors propose a compensation architecture for CT $\Delta\Sigma$Ms based on variable-structure control techniques offering soft-resetting as a better alternative to the conventional resetting presented in Au and Leung (1997). However, it requires the restrictive assumption of infinite sampling rate for stability. The hybrid integrator in Shim, et al. (2005), combining analog and digital integrators, utilizes an adaptive calibration scheme to adjust the digital integrator coefficients for minimizing the in-band noise and distortion.

In this paper, we use a standard model of a modulator, consisting of a continuous-time (leaky) integrator, and a single-bit quantizer. To increase the DR, while avoiding overload, we introduce a local feedback inspired by the anti-windup (AW) control technique (Hu et al, (2002), Grimm et al. (2003) and Galeani et al. (2009)) that mitigates overloading effects without aggressive signal scaling, resulting in a higher dynamic range (DR).

Here through modeling and simulation results, we show how the integrator overloading can be avoided and the resulting SNDR degradation can be improved. At each stage of the loop, relying on well known Lyapunov function based techniques, bounds are obtained to show the performance of the loops with saturation and anti-windup elements. For large modulator inputs, the AW-compensated integrator eliminates the need for digital integrators and additional cancellation filters used in Au and Leung (1997), as well as the infinite sampling rate assumption made in Zourntos and Johns (2002). For higher-order $\Delta\Sigma$Ms, we place an overload prevention (OLP) element after each integrator in order to avoid voltage overload throughout the circuit. For simplicity, and to focus on overloading problem and its mitigation, for results shown here, we use a second-order single-loop $\Delta\Sigma$ modulator with a single-bit quantizer, as in Figure 1.

In Section 2 we discuss the behavioral model of typical integrators in a $\Delta\Sigma$ modulator, while the effects of integrator overload on power spectral density (PSD) and signal-to-noise and distortion ratio (SNDR) are discussed in Section 3. There, the overload region is determined, and the OLP (overload protection) function is introduced to prevent the integrator output from exceeding the overload threshold level. Section 4 describes the proposed compensated integrator, incorporating an AW feedback technique for alleviating the overload shortcoming. Section 5 provides the simulation results of the compensated modulator.

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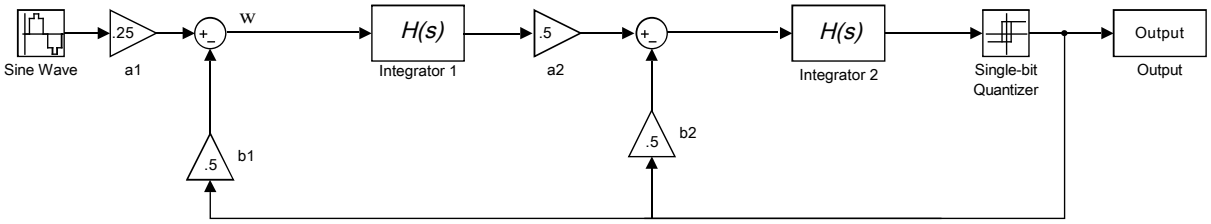

Fig. 1. The scaled second-order single-loop ΔΣM model in SIMULINK including leakage. The single-bit quantizer realized by a relay denoting offset and hysteresis non-idealities.

2. INTEGRATOR MODELING

We rely on Gerfers, et al. (2003) for a simple integrator model to use in the ΔΣ modulator simulations. The finite dc gain of the operational amplifier (opamp) of the CT integrator, also known as leaky integrator, causes integrator gain error (α) and a shift in the pole displacement (γ). The transfer function of the leaky integrator can be expressed as Gerfers, et al. (2003)

$$H(s) = \frac{f_s A_0}{s(1+A_0)+f_s} = \frac{\alpha f_s}{s+\gamma}, \qquad (1)$$
$$\alpha = \frac{A_0}{1+A_0}, \quad \gamma = \frac{f_s}{1+A_0},$$

where f_s is the sampling frequency, and A_0 is the dc gain of the op-amp. The rest of the paper uses the integrator transfer function given by (1). Note that while, consistent with standard practice, we refer to this as the (leaky) integrator model, the model is indeed a stable transfer function with one pole slightly to the left of the imaginary axis.

Figure 1 shows the block diagram of a second-order single-loop ΔΣ modulator with single-bit quantizer to obtain the discrete data, with sampling frequency of f_s (similar to Malkovati et al. (2003) and Zare-Hoseini et al. (2005)). The entire model consists of two (leaky) integrators, two feedback DACs in the feedback loops, and the scaling loop coefficients a_1, a_2, b_1, b_2 to stabilize the loop. The Relay block from SIMULINK is used for the single-bit quantizer (or comparator), which consists of input offset and hysteresis non-idealities. The modulator parameter and coefficient values used in Fig. 1 are summarized in Table 1, where the coefficients are optimized for achieving the best possible signal-to-noise ratio (SNR). As a practical realization, a higher-order modulator architecture could be used to get much lower oversampling ratio (OSR) and sampling frequency f_s, thus minimizing the power consumption of the target ΔΣ modulator. To focus on the core idea here, we rely on the second-order architecture. The technique proposed has immediate application to higher-order models as the modifications needed for each stage are calculated independently.

Table 1. Optimal coefficients and system parameters.

Coefficient	Value	Parameter	Value
A_0	200	Signal bandwidth	$BW = 10.24$kHz
a_1	0.25	Sampling frequency	$f_s = 16.384$MHz
a_2	0.5	Input frequency	$f_{in} = 1.75$kHz
$b_1 = b_2$	0.5	Oversampling ratio	$OSR = 800$
		Number samples	$N = 65536$
		Supply Voltage	$V_{max} = 1.0$V

The effect of finite op-amp gain A_0 on the modulator PSD and SNDR is shown in Fig. 2. It is clear that finite dc gain causes a shift of the PSD knee (which is equal to $\gamma \approx f_s/A_0$) away from dc, resulting in higher baseband noise floor. Accordingly, the PSD knee is displaced to 328 kHz, 82 kHz, and 33 kHz for dc gain of 50, 200, 500, respectively. In the rest of the paper we consider $A_0 = 200$.

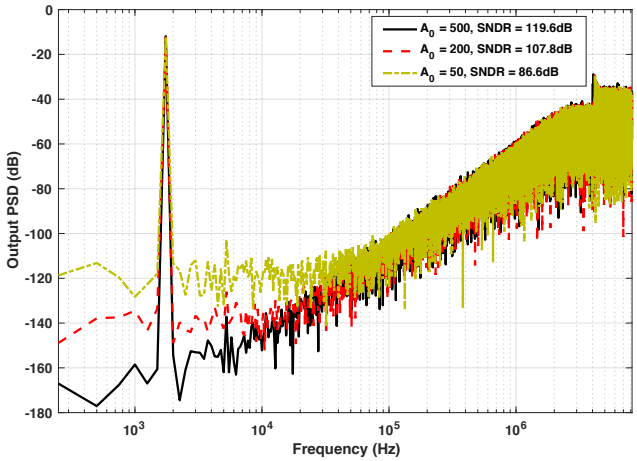

Fig. 2. Effect of finite op-amp dc gain A_0 on PSD and SNDR.

3. MODULATOR'S OVERLOADING

The single-bit quantizer used for the second-order ΔΣM demonstrates a sigmoidal characteristic (Norsvorthy, et al. (1997)), *i.e.*, it exhibits reduced gain when the amplitude of its input is large. Therefore, this nonlinear behavior imposes large harmonic distortion within the frequency band of interest, limiting the SNDR. Such a ΔΣM is subject to what is at times called instability; *i.e.*, severe deterioration in its performance, when the modulator input amplitude exceeds a value, often referred to as the modulator overloading. When the quantizer is overloaded due to a large integrator output, the modulator output no longer increases linearly with the input signal, and the SNDR drops substantially and cannot be restored to its previous value even if the input amplitude reduces to its previous state (Norsvorthy, et al. (1997)). Typically, this necessitates reducing the input voltages to the modulator and thus limiting its dynamic range, below its designed range. To avoid severe performance degradation, the design proposed here employs a novel technique which ensures that the quantizer input (or equivalently the last integrator's output) remains sufficiently below modulator supply voltage (V_{max}), and/or more specifically below the quantizer overloading level (which will be discussed later).

3.1 Overload Detection

In a ΔΣM the modulator input amplitude range is typically given as $[0,\ V_{FS}/2]$, where V_{FS} is the full-scale (peak-to-peak) amplitude (i.e., [0,0.5] for sinewaves whose

peak-to-peak range is between -0.5 and 0.5). Figure 3 plots the modulator SNDR versus the input sinusoidal signal amplitude in dB full scale (dBFS). The overloading phenomena starts when the modulator input (sinusoid) amplitude approaches, but is below, $V_{FS}/2$. As a result, the nonlinear distortion within the signal bandwidth (dc to 10.24 kHz here) increases, and a significant drop in the SNDR occurs. In Fig. 3 the maximum SNDR value in dB before significant drop is labeled as SNDR_{peak} and the modulator input signal level 3dB below that is often referred to as the overload level of the $\Delta\Sigma$M (Yao, et al. (2006)). As can be seen from Fig. 3, the overload condition starts when the voltage of the modulator input goes beyond 0.5V (or -6 dBFS), which corresponds to 0.6V at the integrator output. Consistent with the rest of the analyses in the paper, we denote this level V_{OL} = 0.6V. When input signal amplitude is greater than 0.5V, the integrator output signal goes beyond 0.6V and the peak SNDR starts dropping drastically. When the input amplitude is equal to V_{max} - i.e., the supply voltage (1V or 0 dBFS) - SNDR is only 60 dB, which is 38 dB lower than the peak SNDR.

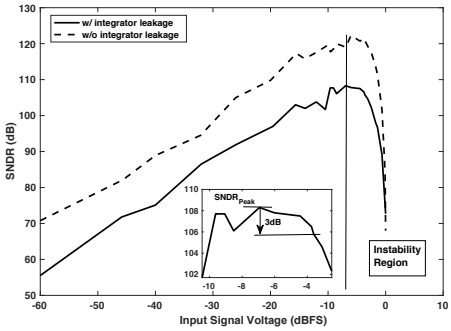

Fig. 3. Estimating modulator overload voltage using SNDR curve for both leaky integrator with $A_0 = 200$ and ideal non-leaky integrator with $A_0 = 10000$.

The core idea of this paper is to reduce this SNDR degradation for input signal amplitudes greater than 0.5V but less than $V_{max} = 1.0$V, which is the maximum possible voltage in the circuit. Moreover, the simulation results for both leaky integrator with A_0 equal to 200 (46 dB), and an almost non-leaky (near-ideal) integrator with A_0 equal to 10,000 (80 dB), are included in Fig. 3 to show a clear distinction between performance deterioration due to the overloading phenomenon and finite op-amp dc gain (or integrator leakage). In both cases, the second-order modulator gets overloaded. The rest of paper considers a realistic model of the leaky integrator with $A_0 = 200$.

3.2 Overload Prevention

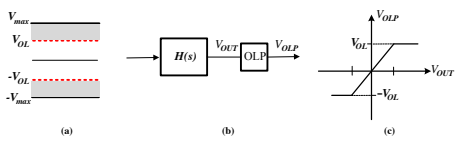

Fig. 4. Proposed integrator: (a) graphical representation of overload region, (b) addition of OLP element, and (c) input-output transfer characteristic of the OLP function.

The approach is graphically illustrated in Fig. 4(a). When integrator output enters the gray zone (between 0.6V and the supply voltage of 1V), the modulator is prone to instability (i.e., severe performance degradation).To increase the DR yet allowing for large signal scaling coefficients (Table I), the proposed approach, shown in Fig. 4(b), employs an overload prevention (OLP) function, which prevents the leaky integrator output from entering the overload region (gray zone), thus avoiding performance degradation (the so called instability). A simple scheme is to add a standard saturation (i.e. OLP) element after the integrator to limit the voltage. The overload voltage estimated from Fig. 3 is used here as V_{OL} (i.e., 0.6V). The OLP (saturation) element ensures that the integrator's output does not go above V_{OL}.

OLP, without further refinement, however, creates significant harmonic distortion within the desired bandwidth at the output PSD and causes major SNDR degradation. To investigate the effects of OLP on the $\Delta\Sigma$M's PSD and SNDR, an overload factor, K_{OL}, is introduced to represent how much the integrator input is increase beyond the safe range (Fig. 4(a)). The K_{OL} factor is defined as the ratio of input signal amplitude at $SNDR_{peak}$, which is 0.5V, and the current input signal amplitude. For example, $K_{OL} = 1$ corresponds to no overload condition (inactive OLP) while $K_{OL} = 0.67$ corresponds to the input amplitude of 0.75V causing a 50% increase in dynamic range (note, $0.5 \leq K_{OL} \leq 1$, due to supply voltage of 1V).

Figure 5 shows the effect of OLP (or saturation limit) on output PSD and the resulting odd-order in-band harmonic distortion for various K_{OL} values. The OLP element, used without further modification, causes third- and fifth-order harmonic distortion to grow larger as K_{OL} gets smaller. A smaller K_{OL} factor means more aggressive overload near V_{max}. For instance, for $K_{OL} = 0.56$, the artificial saturation introduced by the OLP block increases the HD3 value from -112.5dB to -74.4dB and the HD5 value from -117.1dB to -79.1dB. As a result, SNDR, as a crucial quality measure of a $\Delta\Sigma$M, degrades from 105.5dB to 73.2dB, which is unacceptable in many applications.

To summarize, the OLP function introduces harmonic distortion at the desired low frequencies of the PSD, which is not desirable. Thus, while insertion of an OLP or saturation element after integrator may avoid overload issue, if left unmitigated by the proposed AW approach will cause severe performance degradation.

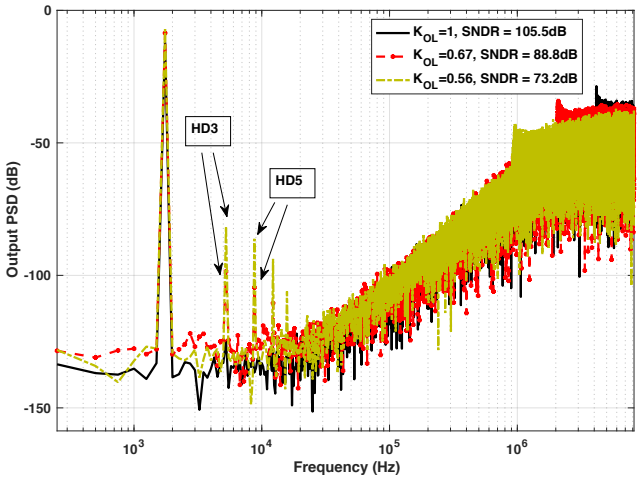

Fig. 5. Effect of OLP function (or saturation element) on PSD and SNDR. All integrators are considered as real leaky integrator with finite dc gain $A_0 = 200$.

4. ANTI-WINDUP DESIGN

An augmentation technique, inspired by the anti-windup design, is proposed for the internal loops in order to minimize the effects of the shortcoming of a standalone OLP discussed in Section 3.2. Roughly speaking, the AW feedback suppresses the integrator input amplitude whenever its output exceeds V_{OL} and remains inactive otherwise.

To meet the closed-loop structure that is needed for anti-windup design, a feedback with a small gain α_a is added to the leaky integrator $H(s)$ following the OLP block, as shown in Fig. 6. It is important to ensure that the added feedback branch has a negligible impact on the overall system performance. Therefore, the modulator is simulated with and without α_a branch, and the resulting PSDs are shown in Fig. 7, validating negligible SNDR change (less than 1dB) when the artificial leakage α_a is chosen as 0.0002.

This slight modification turns the second-order modulator schematic shown in Fig. 1 into the re-arrangement shown in Fig. 8 which is ready for AW augmentation, while Figure 9 depicts the standard configuration for anti-windup design for each $H(s)$, which is denoted by C (see below).

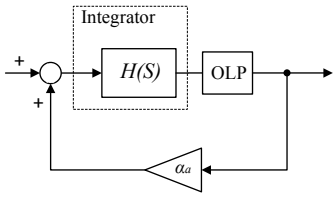

Fig. 6. Overload-prevented integrator with very small artificial leakage α_a equal to 0.0002.

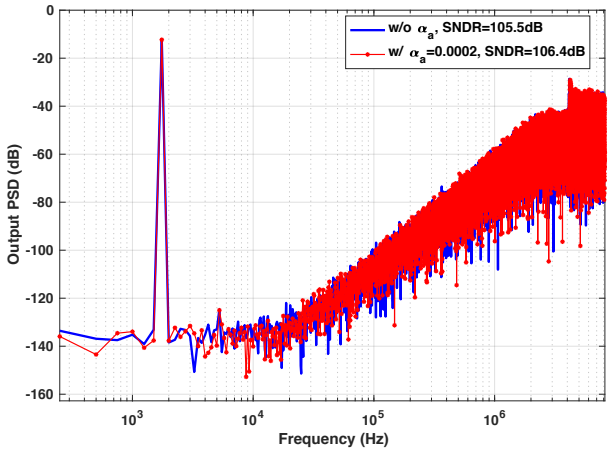

Fig. 7. Negligible effect of $\alpha_a = 0.0002$ on PSD and SNDR.

Next, we show how the block diagram in Fig. 6 could now be interpreted as a control feedback loop for the standard AW design shown in Fig. 9 where block C here corresponds to the leaky integrator $H(s)$ with transfer function $\frac{\alpha f_s}{s+\gamma}$ followed by OLP (or saturation) in Fig. 6 whereas the plant P corresponds to a simple unity-gain connection in Fig. 6. The AW compensation feedback is then added in Fig. 9 in order to minimize the overload effects.

Fig. 9(bottom) illustrates a possible realization of the designed AW feedback loop with a minimal hardware complexity, including three 1-bit comparators, two XOR gates and three switches that control the AW feedback gain. The implementation strategy is such that we divide the overload region encircled between V_{OL} and V_{max}, shown in Fig. 4(a), into three parts separated by threshold levels V_{OL1}=$(V_{max} - V_{OL})/3$ and V_{OL2}= $2(V_{max} - V_{OL})/3$. The 1-bit comparators constantly monitor the integrator output and determine in what specific local overload region the output voltage is, and then two XOR gates encode the output bits of the comparators in order to control the gates of three switches, which connects the corresponding AW gain to the integrator input for mitigating the overloading issue. Thus, if the integrator does not overload, all switches remain open, so the AW loop is not active. However, if it overloads, based on the level of saturation (slight/moderate/high) only one of the three switches closes and the adjusted signal q is multiplied by the AW gain $-\Lambda$. Note that this schematic is for each $\Lambda_i q$, and two such circuits are needed for each stage. Other possible circuit realizations would be similar to the one used in Moussavi and Leung (1994) or Yu and Tseng (2013).

The state-space realization for each integrator transfer function, with internal state x_c (i.e. integrator state), is

$$\dot{x}_c = A_c x_c + B_{cy} y + B_{cw} w, \quad u = C_c x_c, \tag{2}$$

with w as the input to the integrator and

$$[\, A_c | B_{cy} | B_{cw} | C_c \,] = [\, -\gamma | \alpha_a | 1 | \alpha f_s \,]. \tag{3}$$

As discussed earlier, the integrator output is subject to OLP; *i.e.* $|y| \leq V_{OL}$ with $V_{OL} = 0.6V$.The OLP output y is thus modeled as $y = OLP(u)$ (or simply put $SAT(u)$). As discussed earlier, the addition of the OLP block alone does not improve the performance. The objective here is to design an augmentation that introduces suitable additive signals v_s and v_u to the state dynamics and output of the unconstrained controller (2), respectively

$$\begin{aligned} \dot{x}_c &= A_c x_c + B_{cy} y + B_{cw} w + v_s, \\ u &= C_c x_c + v_u. \end{aligned} \tag{4}$$

Following the standard approach in anti-windup design (Reineh, et al. (2018) or Grimm et al. (2003)), the error between the input and output of the OLP element, q, is used to generate anti-windup compensation, with SIMULINK modulator model shown in Fig. 9, where ν_s, ν_u are shown as ν_1, ν_2 for each $H(s)$. The vector signal v in (4) ($v = [v_s \quad v_u]^\top$) is then $v = -\Lambda q$ with $\Lambda = [\Lambda_s \quad \Lambda_u]^\top$.

Substituting $y = u - q$ in (4), it is straightforward to build the closed-loop system with state x_c, and w and q as input signals. The closed-loop system with anti-windup gains can be written as

$$\begin{aligned} \dot{x}_c &= (A_c + B_{cy} C_c) x_c + B_{cw} w - ([1 \quad B_{cy}]\Lambda + B_{cy}) q, \\ u &= C_c x_c - [0 \quad 1]\Lambda q, \end{aligned} \tag{5}$$

with y to be the performance measurement and $A_0 = 200$, $\alpha_a = 0.0002$. The AW gain Λ is obtained using the convex optimization algorithm presented in Theorem 1 below.

Theorem 1. (**Anti-windup Design: Integrator stability**)
Consider the block diagram shown in Fig. 9 with a unity-gain for plant P and the integrator (2) as the nominal controller C. Then, given the OLP function shown in Fig. 4, there exists a solution for the convex minimization problem: If

$$\min_{Q,M,X,\chi} \quad \chi \tag{6}$$

subject to the linear matrix inequality

$$\begin{pmatrix} 2Q(A_c + B_{cy}C_c) & * & * & * \\ B_{cw} & -\chi & * & * \\ C_c Q & 0 & -\chi & * \\ \Phi_{4,1} & 0 & -X^\top [0 \quad 1]^\top - M & \Phi_{4,4} \end{pmatrix} < 0, \tag{7}$$

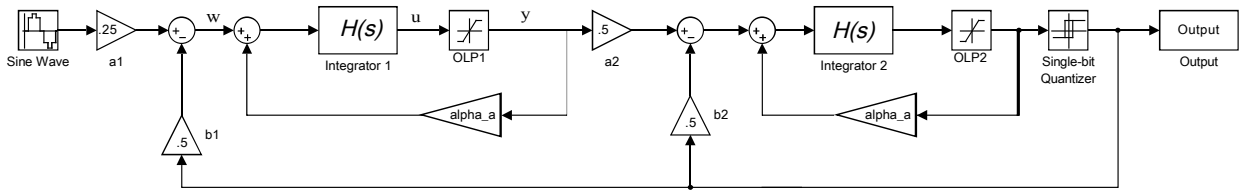

Fig. 8. The scaled second-order single-loop ΔΣM model in SIMULINK with artificial leakage.

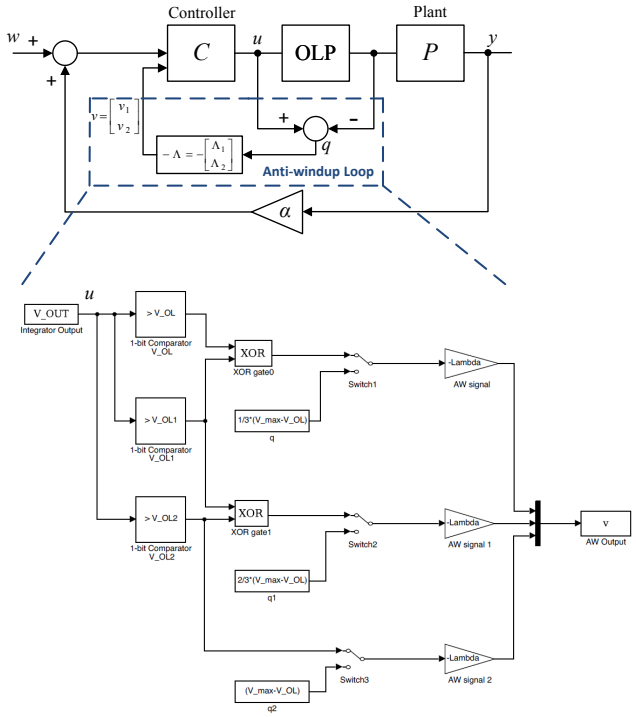

Fig. 9. A generic anti-windup diagram consisting of blocks C and P representing controller and plant, respectively (top). A simplified model of the designed AW in the form of the circuit-like realization (bottom).

with scalar M,

$$X = \Lambda M \tag{8}$$

and

$$\Phi_{4,1} = -X^\top [1 \quad B_{cy}]^\top - MB_{cy} + C_c Q, \tag{9}$$
$$\Phi_{4,4} = -2M - [0 \quad 1]X - X^\top [0 \quad 1]^\top.$$

then, the closed-loop system (5), which is one stage of the modulator, using anti-windup gain

$$\Lambda = XM^{-1}, \tag{10}$$

is stable with a gain χ from its input to its output.

Proof. Consider a quadratic Lyapunov function

$$V = Q^{-1}x_c^2, \tag{11}$$

where x_c is the integrator state, and $Q > 0$ the scalar version of Lyapunov matrix. By applying the Schur compliment followed by a congruent transformation the inequality (7) can be written as

$$\frac{d}{dt}(Q^{-1}x_c^2) + \chi^{-1}y^2 - \chi w^2 - 2qW(q-u) < 0, \tag{12}$$

where $W = M^{-1}$, u is the output of the integrator, and q is the error between u and the output of the OLP block. Using the definition of OLP nonlinearity (Fig. 4), the following sector condition holds

$$2qW(q-u) \geq 0, \tag{13}$$

with $W > 0$ as a scaling variable. Given (13) , inequality (12) reduces to

$$\dot{V} + \chi^{-1}y^2 - \chi w^2 < 0. \tag{14}$$

Without w, this establishes stability, and with w and zero initial conditions it ensures stability with performance measure χ. □

The anti-windup design requires the unconstrained closed-loop system to be stable; i.e. the coefficient multiplying x_c on the right-hand side of (5) should have a strictly negative eigenvalue. After substituting the values shown in (3), this coefficient is given by

$$A_c + B_{cy}C_c = -\gamma + \alpha_a \alpha f_s, \tag{15}$$

which is stable for $\alpha_a < 1/A_0$.

Unlike standard AW cases where the results are often necessary conditions, the wording of Theorem 1 implies feasibility. This is due to the special structure of the model. Given closed-loop stability, there exists a $Q > 0$ for a sufficiently large χ (bounded real inequality). This Q would also satisfy the open loop version of the bounded real inequality. Satisfying both is the feasibility condition (Grimm, et al., 2003). This results established that each individual loop (around one $H(s)$ is well behaved. Optimizing χ leads to an aggressive AW gain, which helps reduce input to $H(s)$ is its output goes above V_{OL} of 0.6V.

5. SIMULATION RESULTS

The block diagram of the DSM with AW is shown in Fig. 10. If stages are identical, the gains Λ_i for each stage would be the same as other stages and only one set is needed to be calculated. Results are presented for 0.75V input signal amplitude (50% higher than $SNDR_{peak}$ input), corresponding to $K_{OL} = 0.67$. The overload voltage $V_{OL} =$ 0.6V estimated in Section 3.1 is used for the OLP function. The AW gain $\Lambda_1 = \Lambda_2 = [-0.01, 1.03]^\top$ is obtained from Matlab convex optimization tools satisfying stability and performance constraints in Theorem 1.

Figure 11 shows the PSD of the system when the output of the integrators are subject to OLP with $\pm V_{OL}$ and modulator input has amplitude of 0.75. For this considerable level of overload, the proposed AW technique has achieved only 1dB drop from $SNDR_{peak}$ while ensuring performance for almost 50% larger input amplitudes ($K_{OL} = 0.67$). Note also, using AW, the third and fifth harmonic distortions have been significantly reduced. Therefore, the AW augmentations have significantly improved the performance of the modulator with OLP while maintaining the stability by reducing the quantizer input and avoiding its overload. This shows that the anti-windup compensated system is able to increase the dynamic range of the modulator and accommodate larger input signals safely, without overloading the integrator.

6. CONCLUSION

A compensated integrator using an anti-windup feedback technique was proposed to extend the dynamic range of

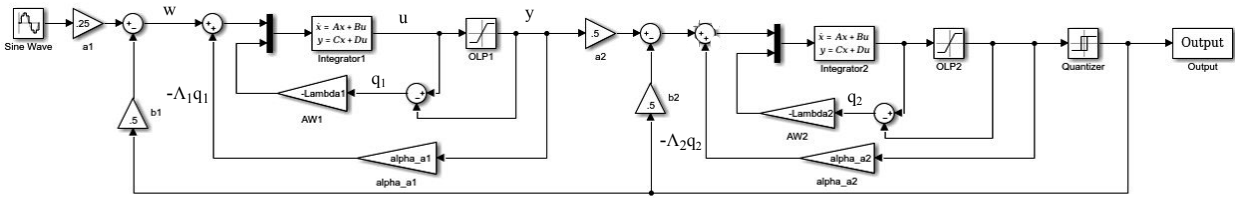

Fig. 10. Behavioral model of a second-order delta-sigma modulator including anti-windup compensation feedback.

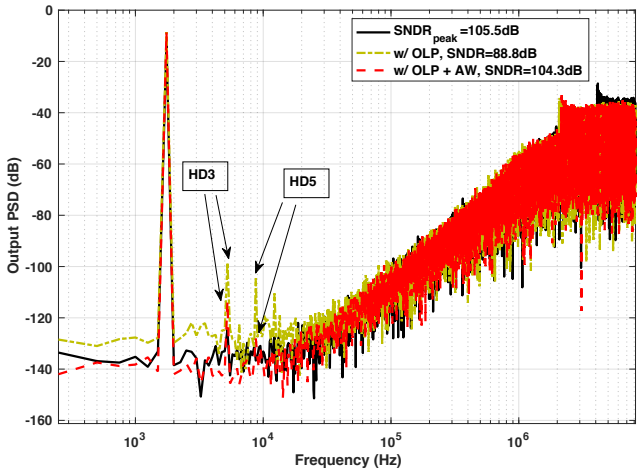

Fig. 11. Effect of AW on PSD and SNDR with $K_{OL} = 0.67$.

$\Delta\Sigma$ modulators by avoiding integrator overload. Using an anti-windup approach, SNDR cam be retrieved close to its peak value while accommodating a 50% higher dynamic range. The gains for each integrator stage is obtained separately and depends on the specifications of the blocks in that stage (i.e. A_o, etc). If all stages are identical, only one set needs to be obtained.

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