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Stability of charge-pump phase-locked loops: the hold-in and pull-in ranges

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Abstract: The problem of design and analysis of synchronization control circuits is a challenging task for many applications: satellite navigation, digital communication, wireless networks, and others. In this article the Charge-Pump Phase-Locked Loop (CP-PLL) electronic circuit, which is used for frequency synthesis and clock generation in computer architectures, is studied. Analysis of CP-PLL is not trivial: full mathematical model, rigorous definitions, and analysis still remain open issues in many respects. This article is devoted to development of a mathematical model, taking into account engineering aspects of the circuit, interpretation of core engineering problems, definition in relation to mathematical model, and rigorous analysis.

Keywords: CP-PLL, charge-pump, phase-locked loops, phase-frequency detector, PFD, hold-in range, pull-in range, control of phase synchronization, nonlinear analysis,

1. INTRODUCTION

Design and analysis of frequency control circuits is a challenging task relevant to many applications: satellite navigation (Kaplan and Hegarty, 2006), digital communication (Proakis and Salehi, 2008), wireless networks (Du and Swamy, 2010), to mention just a few. Effective locking onto the phase of the input signal is among the principal problems solved by means of such circuits. From a broad perspective, their synthesis and analysis fall under the framework of standard topics in control engineering like signal tracking, linear and global stability. Meanwhile, some of ubiquitous and actively used circuits are largely inspired by implementability issues and approaches of practical control engineering so that their true capacities and limitations still await fully disclosing via a rigorous analysis.

This paper aims at filling this gap with respect to the Charge-Pump Phase-Locked Loop (CP-PLL), which is used for frequency synthesis and clock generation in computer architectures (Bianchi, 2005). Stability of the CP-PLL steady state was originally studied in (Gardner, 1980) using approximate linear models. Later on, approximate discrete-time linear models of the CP-PLL were suggested in (Hein and Scott, 1988; Lu et al., 2001). The closed loop nonlinear discrete time model of CP-PLL was suggested in (Van Paemel, 1994) and then some gaps in were filled in (Kuznetsov et al., 2019c). In this paper, we develop, augment, and supplement the approach used in the reported literature in order to extend it to the practically important case of Voltage Controlled Oscillator (VCO) overload (see, e.g. (Gillespie et al., 2000; Kuznetsov et al., 2019b)).

The range of input frequencies associated with stable steady state corresponds to the hold-in range. For the classical analog PLL, stability of the locked state depends on the gap between the VCO free-running frequency and the frequency of the reference signal. For active proportionally-integrating (PI) filter, analog PLL is theoretically stable for any gap. Conversely, stability of the steady state of CP-PLL depends on the reference frequency even if PI loop filter is employed. Moreover, the CP-PLL is stable only for relatively high input frequencies, which situation is far different from that with stability of analog PLLs. It follows that even the definitions of the hold-in, the pull-in and the lock-in ranges (see, e.g. (Kuznetsov et al., 2015; Leonov et al., 2015; Best et al., 2016; Kuznetsov et al., 2019a)) should be refined for the CP-PLL, to say nothing about the need to update and extend the base of relevant knowledge about the properties of the circuit.

Extra troubles stem from the fact that straight-forward linearisation of available CP-PLL models may lead to incorrect conclusions, because the system is not smooth near the steady state (in fact, it is only piecewise smooth). In (Curran et al., 2013), stability analysis follows the lines of a Lyapunov approach, however, details of the proof are not presented.

In this paper, we use the findings of (Kuznetsov et al., 2019c) as a keystone, and develop, augment, and supplement them in order to acquire a fairly complete mathematical model of CP-PLL reliable enough to serve as a tool for credible analysis of dynamical properties of these circuits. To this end, we also refine some relevant mathematical definitions of main characteristics, and demonstrate the potentiality of the proposed model.

2. MATHEMATICAL MODEL OF CP-PLL

Consider the charge-pump phase-locked loop with phase-frequency detector (Gardner, 1980, 2005) in Fig. 1. Both the reference (Ref) and output of the VCO are square waveform signals. Without loss of generality we suppose that trailing

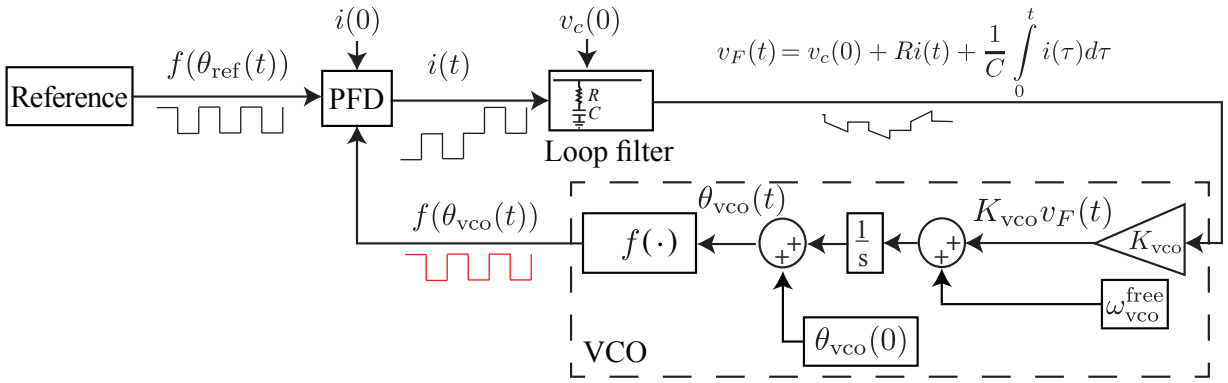

Fig. 1. Charge-pump phase-locked loop with phase-frequency detector (Charge-pump PLL)

edges of the VCO and reference signals occur when the corresponding phase reaches an integer number. The frequency ω_{ref} of reference signal (reference frequency) is usually assumed to be constant:

$$\theta_{\text{ref}}(t) = \omega_{\text{ref}} t = \frac{t}{T_{\text{ref}}}, \tag{1}$$

where T_{ref}, ω_{ref} and $\theta_{\text{ref}}(t)$ are a period, frequency and a phase of the reference signal.

The Phase-Frequency Detector (PFD) is a digital circuit, triggered by the trailing (falling) edges of the reference Ref and VCO signals. The output signal of PFD $i(t)$ can have only three states (Fig. 2): 0, $+I_p$, and $-I_p$. To construct a mathematical

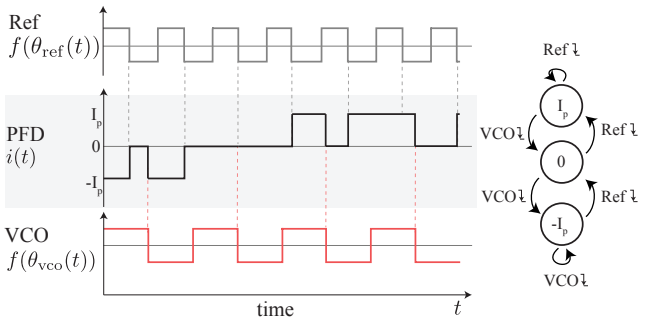

Fig. 2. Phase-frequency detector operation.

model, we wait for a trailing edge of the reference signal and define the corresponding time instance as $t = 0$. Suppose that before $t = 0$ the PFD had a certain constant state $i(0-)$. A trailing edge of the reference signal forces the PFD to switch to a higher state, unless it is already in the state $+I_p$. A trailing edge of the VCO signal forces the PFD to switch to a lower state, unless it is already in the state $-I_p$. If both trailing edges happen at the same time, then the PFD switches to zero.

Thus, $i(0)$ is determined by the values $i(0-)$, $\theta_{\text{vco}}(0)$, and $\theta_{\text{ref}}(0)$. Similarly, $i(t)$ is determined by $i(t-)$, $\theta_{\text{vco}}(t)$, and $\theta_{\text{ref}}(t)$. Thus, $i(t)$ is a piecewise constant and right-continuous.

The relationship between the input current $i(t)$ and the output voltage $v_F(t)$ for a proportionally integrating (perfect PI) filter based on resistor and capacitor is as follows

$$v_F(t) = v_c(0) + Ri(t) + \frac{1}{C}\int_0^t i(\tau)d\tau,\ H(s) = R + \frac{1}{Cs}, \tag{2}$$

where $R > 0$ is a resistance, $C > 0$ is a capacitance, and $v_c(t) = v_c(0) + \frac{1}{C}\int_0^t i(\tau)d\tau$ is a capacitor charge.

The control signal $v_F(t)$ adjusts the VCO frequency:

$$\dot{\theta}_{\text{vco}}(t) = \omega_{\text{vco}}(t) = \omega_{\text{vco}}^{\text{free}} + K_{\text{vco}} v_F(t), \tag{3}$$

where $\omega_{\text{vco}}^{\text{free}}$ is the VCO free-running (quiescent) frequency (i.e. for $v_F(t) \equiv 0$), K_{vco} is the VCO gain (sensivity), and $\theta_{\text{vco}}(t)$ is the VCO phase.

Consider one important thing regarding the charge-pump (CP) using in the PFD: transistors inside CP reasonably approximates the current generators until the drain-source voltage magnitude is higher than a given minimum value. Note that both transistors' output characteristics approximate the current generators only if the output voltage is within the current saturation region. The CP-PLL will work as expected only if the CP output voltage is within its valid range. In order to keep both transistors within their current saturation region, a "zero impedance" (or very low) to ground (or to any DC voltage) is needed. This means that the loop filter has to have a capacitor to GND if it is purely passive. The simplest solution is a second-order filter, which will be considered in future publications. Another solution is to add operational amplifier to the filter. In this case the transfer function of the loop filter remains the same.

If the CP-PLL is used to make a frequency synthesizer [1], then the loop also includes a variable frequency divider. In many cases (output frequency above some hundred MHz) the first stage of the frequency divider is a prescaler or a dual modulus prescaler. This component, without any input signal, normally oscillates at a frequency, which slightly higher than its maximum working range. Therefore if the VCO is not oscillating, then it oscillates the prescaler: the CP-PLL "understands" that the VCO frequency is too high, pushing the tuning voltage as down as possible. If at the CP-PLL switch-on (most probably the tuning voltage is zero or very low) the VCO is not oscillating, it will never oscillates and the CP-PLL never locks.

The CP-PLL is also used without frequency divider in order to provide a local clock signal phase-coherent with an external reference [2]. In that case the VCO is a tunable quartz oscillator, with very limited tuning range, and the initial frequency is most probably well in the pull-in range. The probability that the VCO frequency is inside the lock-in range is low since the

[1] 99% of the applications in Advantest Corporation.
[2] 1% of the applications in Advantest Corporation.

synchronous-clock-PLL has normally a very narrow CP-PLL bandwidth: from few Hz to some hundreds of Hz.

Further we assume that there is no prescaler and the VCO input may experience overload. From the mathematical point of view it means that $\dot{\theta}_{\rm vco}(t)$ may become zero at some point (the VCO overload).

From (1), (2), and (3), for given $i(0-)$ and $\omega_{\rm ref}$ we obtain a *continuous time nonlinear mathematical model of CP-PLL* described by the following differential equations

$$\dot{v}_c(t) = \tfrac{1}{C} i(t), \quad \dot{\theta}_{\rm vco}(t) = \omega_{\rm vco}^{\rm free} + K_{\rm vco}\left(Ri(t) + v_c(t)\right) \tag{4}$$

with the following discontinuous piecewise constant nonlinearity $i(t) = i\big(i(t-), \omega_{\rm ref}, \theta_{\rm vco}(t)\big)$ and the initial conditions $\big(v_c(0), \theta_{\rm vco}(0)\big)$. This model is nonlinear, non-autonomous, discontinuous, switching system, which is hard to analyze.

2.1 Locked states

If the synchronization is achieved, i.e. transient process is over, then the loop is said to be in a *locked state*. The CP-PLL is in a locked state if the trailing edges of the VCO signal happen almost at the same time as the trailing edges of the reference signal. In a locked state the output of PFD $i(t)$ can be non-zero only on short time intervals (shorter than $\tau_{\rm lock}$). The allowed residual phase difference $\tau_{\rm lock}$ should be in agreement with engineering requirements for a particular application. We consider the ideal case $\tau_{\rm lock} = 0$. In practice, the locked state should be outside of the overload zone of VCO, i.e. $\dot{\theta}_{\rm vco}(t) > 0$ must be satisfied. For nonlinear analysis, we pass from model (4) to a discrete-time model.

3. NONLINEAR DISCRETE TIME CP-PLL MODEL

Following (Kuznetsov et al., 2019c), we consider a discrete time model of the CP-PLL. Let $t_0 = 0$. Denote by $t_0^{\rm middle}$ the first instant of time such that the PFD output becomes zero. If $i(0) = 0$, then $t_0^{\rm middle} = 0$. Then we wait until the first trailing edge of the VCO or Ref, and denote the corresponding moment of time by t_1. Continuing in a similar way, one obtains increasing sequences $\{t_k\}$ and $\{t_k^{\rm middle}\}$ for $k = 0, 1, 2....$

Let $t_k < t_k^{\rm middle}$. Then for $t \in [t_k, t_k^{\rm middle})$ the sign $(i(t))$ is a non-zero constant (± 1). Denote by τ_k the PFD pulse width (length of the time interval, where the PFD output is a non-zero constant), multiplied by the sign of the PFD output (see Fig. 3):

$$\begin{aligned} &\tau_k = \left(t_k^{\rm middle} - t_k\right) \operatorname{sign}\left(i(t)\right), \quad t \in [t_k, t_k^{\rm middle}), \\ &\tau_k = 0 \qquad\qquad\qquad\qquad\quad t_k = t_k^{\rm middle}. \end{aligned} \tag{5}$$

If the VCO trailing edge hits before the Ref trailing edge, then $\tau_k < 0$ and in the opposite case we have $\tau_k > 0$. Thus, τ_k shows how one signal lags behind another.

From (2) it follows that the zero output of PFD $i(t) \equiv 0$ on the interval $(t_k^{\rm middle}, t_{k+1})$ implies a constant filter output. Denote this constant by v_k. We have

$$v_F(t) \equiv v_k, \quad t \in [t_k^{\rm middle}, t_{k+1}). \tag{6}$$

Following the ideas from (Acco, 2003; Curran et al., 2013), the number of parameters can be reduced to just two (α and β):

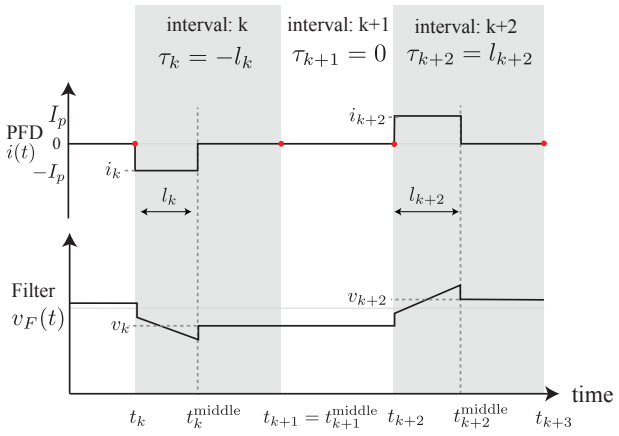

Fig. 3. Discrete states τ_k and v_k (l_k is the PFD pulse width).

$$\begin{aligned} &p_k = \frac{\tau_k}{T_{\rm ref}}, \; u_k = T_{\rm ref}\left(\omega_{\rm vco}^{\rm free} + K_{\rm vco} v_k\right) - 1, \\ &\alpha = K_{\rm vco} I_p T_{\rm ref} R, \; \beta = \frac{K_{\rm vco} I_p T_{\rm ref}^2}{2C}. \end{aligned} \tag{7}$$

Here p_k is a normalized phase shift and $u_k + 1$ is a ratio of the VCO frequency $\omega_{\rm vco}^{\rm free} + K_{\rm vco} v_k$ to the reference frequency $\frac{1}{T_{\rm ref}}$. Final system of equations describing CP-PLL without overload is the following (Kuznetsov et al., 2019c)

$$u_{k+1} = u_k + 2\beta p_{k+1},$$

$$p_{k+1} = \begin{cases} \dfrac{-(u_k+\alpha+1) + \sqrt{(u_k+\alpha+1)^2 - 4\beta c_k}}{2\beta}, \\ \qquad \text{for } p_k \geq 0, \quad c_k \leq 0, \\ \dfrac{1}{u_k+1} - 1 + (p_k \bmod 1), \\ \qquad \text{for } p_k \geq 0, \quad c_k > 0, \\ l_k - 1, \quad \text{for } p_k < 0, \quad l_k \leq 1, \\ \dfrac{-(u_k+\alpha+1) + \sqrt{(u_k+\alpha+1)^2 - 4\beta d_k}}{2\beta}, \\ \qquad \text{for } p_k < 0, \quad l_k > 1, \end{cases} \tag{8}$$

where

$$\begin{aligned} &c_k = (1 - (p_k \bmod 1))(u_k + 1) - 1, \\ &S_{l_k} = -(u_k - \alpha + 1) p_k + \beta p_k^2, \\ &l_k = \frac{1 - (S_{l_k} \bmod 1)}{u_k + 1}, \; d_k = (S_{l_k} \bmod 1) + u_k. \end{aligned}$$

One of the advantages of (8) is that it has the only one steady state at $(u_k = 0, p_k = 0)$. For practical purposes, only *locally (asymptotically) stable steady state*, in which the loop returns after small perturbations of its state, is of interest.

Here the VCO overload conditions have the following form

$$\begin{aligned} &p_k > 0, \; u_k < 2\beta p_k - 1, \\ &p_k < 0, \; u_k < \alpha - 1. \end{aligned} \tag{9}$$

If conditions (9) are satisfied, then the additional cases of the loop dynamics have to be taken into account (see (Kuznetsov et al., 2019c,b)).

In practice the VCO overload should be avoided. From the mathematical point of view a task may be posed to find the biggest positively invariable region of phase space in which there is no overload. However for any parameters the VCO overload may occur for sufficiently large frequency difference

between the VCO and reference signals. Therefore it is reasonable to demand that at least in a vicinity of the steady state there is no overload (local lack of the overload). From (Kuznetsov et al., 2019c,b) we get $0 < \alpha < 1$, and this implies the following condition on the period of the input signal

$$T_{\text{ref}} < T_{\text{overload}}^{\text{local}} = (K_{\text{vco}} I_p R)^{-1} \tag{10}$$

It is also necessary to avoid the VCO overload during startup where even if the initial frequencies are equal, the initial phase difference p_0 may take any value from $(-1,1)$. Moreover, the phase difference may change due to a noise and other reasons. Therefore it is reasonable to demand that the VCO is not overloaded for all $-1 < p_0 < 1$ at least for the case of identical VCO and reference frequencies, i.e. for $u_0 = 0$ (nonlocal lack of the overload). These requirements lead to the estimates $0 < \beta < \frac{1}{2}$ and $0 < \alpha < 1$, and it implies the following condition on the period of the input signal

$$T_{\text{ref}} < T_{\text{overload}}^{\text{nonlocal}} = \min\left\{\sqrt{\frac{C}{K_{\text{vco}} I_p}}, \frac{1}{K_{\text{vco}} I_p R}\right\} \tag{11}$$

3.1 Small-signal analysis: the hold-in range

Model (8) has only one steady state

$$u_k = u_{k+1} \equiv 0, \;\; p_k = p_{k+1} \equiv 0, \tag{12}$$

which is a locked state if it is locally asymptotically stable. The hold-in range corresponds to the input frequency range, which allows PLL to keep acquired the locked state despite small and slow deviations of input frequency ω_{ref}. This notion is similar to the definition of the hold-in range for classic analog PLLs for the fixed $\omega_{\text{vco}}^{\text{free}}$ (Kuznetsov et al., 2015; Leonov et al., 2015; Best et al., 2016). However there are two important differences. First, free-running frequency of VCO should not be equal to the frequency of input signal because in this case the charge-pump will not operate properly. Second, for the CP-PLL model considered there is always some reference signal period T_{ref} such that the steady state $u_k = p_k = 0$ is stable (assuming that there is no overload). Moreover, for all smaller values of T_{ref} the equilibrium $u_k = p_k = 0$ remains locally stable. Therefore it is reasonable to give the following definition of the hold-in range for the CP-PLLs.

Definition 1. The hold-in range of the CP-PLL is a maximum range of the input signal periods $T_{\text{ref}} = \frac{1}{\omega_{\text{ref}}}$:

$$0 < T_{\text{ref}} < T_{\text{hold-in}}, \tag{13}$$

such that a locked state (i.e., asymptotically stable steady state) exists and the VCO is not overloaded at this state.

Here $\omega_{\text{vco}}^{\text{free}}$ does not affect the hold-in range and can be predetermined for certainty. Since it is not possible to choose zero value $\omega_{\text{vco}}^{\text{free}} = 0$ (because in this case the transistors inside the charge-pump do not operate properly), one can choose $\omega_{\text{vco}}^{\text{free}} = \frac{1}{T_{\text{hold-in}}}$.

The local stability analysis of the CP-PLL model via straightforward linearisation may lead to incorrect conclusions because the system is not smooth near the steady state (in fact, it is only piecewise smooth). In (Feely, 2007; Curran et al., 2013) the stability analysis follows the lines of the Lyapunov approach, however the details of the proof are not presented [3] and the analysis is done without taking into account the VCO overload (see (9)). In (Kuznetsov et al., 2019c,b, 2020) it is shown that a small vicinity of the steady state lies outside the overload for (10) (thus we can apply (8) for the local analysis of the loop), and using local piecewise smoothness of the right hand-side of model (8) it is proved that the steady state is uniformly exponentially stable if $0 < \beta < 2$, $\beta \neq \frac{3}{2}$. For $\beta = \frac{3}{2}$ the linearization procedure fails, with all orbits settling onto Period 3 cycles. However, simulation suggests that in system (8) these cycles are broken up, becoming slowly decaying spirals. This allows us to estimate the hold-in range, according to Definition 1.

Proposition 1 (the hold-in range of CP-PLL).

$$\frac{1}{\omega_{\text{ref}}} = T_{\text{ref}} < T_{\text{hold-in}} = \min\left\{\sqrt{\frac{4C}{K_{\text{vco}} I_p}}, \frac{1}{K_{\text{vco}} I_p R}\right\}. \tag{14}$$

This value refines the estimate $T_{\text{hold-in}} < \sqrt{\frac{4C}{K_{\text{vco}} I_p}}$ which can be obtained according to Definition 1 from the results in (Curran et al., 2013) without taking into account overload.

3.2 Large-signal analysis: the pull-in range

Unlike classic PLLs with PI filter (Alexandrov et al., 2015; Kuznetsov et al., 2019a), for some parameters and initial input frequencies the CP-PLL may not acquire the locked state due to the presense of nontrivial oscillations (attractors) in the phase-space. For given parameters, the input frequency range for which a locked state is acquired from any possible initial state is known as the pull-in range.

Definition 2. (The pull-in range). The pull-in range of CP-PLL is a maximum range of the input signal periods $T_{\text{ref}} = \frac{1}{\omega_{\text{ref}}}$ within the hold-in range:

$$0 < T_{\text{ref}} < T_{\text{pull-in}} \leq T_{\text{hold-in}}, \tag{15}$$

such that for any initial state the CP-PLL acquires a locked state.

An upper estimate of the pull-in range can be obtained via the analysis of limit cycles. While for the discrete time model (8) the limit cycles of low-periods without overload can be easily found analytically (see, e.g. (Homayoun and Razavi, 2016; Kuznetsov et al., 2020)), the computation of limit cycles of higher periods or with overload lead to complicated equations, which need to be solved numerically.

Note, that for $0 < \beta < 2$, $0 < \alpha < 1$ the steady state is stable, and therefore the existing limit cycles can be classified as hidden oscillations (Leonov and Kuznetsov, 2013). Similar to the classical PLL, the existence of hidden periodic oscillations with higher periods may restrict the pull-in range (for the classical PLL the birth of hidden oscillation without loss of local stability of the stationary set can cause the loss of global stability (hidden boundary of global stability) and restrict the pull-in range (Bianchi et al., 2016; Kuznetsov et al., 2017; Kuznetsov, 2020)).

4. CONCLUSIONS

Although the stability of the Charge-Pump PLL has been studied for a long time, the VCO input overload was not fully taken into account. Also in these studies such standard engineering parameters as the hold-in and pull-in ranges were not introduced and estimated. In this work the definitions of the hold-in

[3] "The proof of this assertion is neither trivial nor brief. Its inclusion would comprise too great a tangent to the narrative of the paper and extend the length beyond what is reasonable." (Curran et al., 2013)

and pull-in ranges for the CP-PLL are introduced in terms of the input signal period and frequency and the corresponding estimations are discussed. We showed that the VCO input overload actually limits the hold-in and pull-in ranges even more than the domains of parameters corresponding to linear stability and non-existence of limit cycles.

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